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electronics today

INTERNATIONAL NOVEMBER 1982 85p

THE BIG ONE!

16-BIT COLOUR COMPUTER TO BUILD!

- Up to 16 serial I/O ports
- UCSD PASCAL on disc
- High resolution graphics
- Powerful resident BASIC
- Separate 16K video RAM
- Addressing up to 1M
- Up to 60K of user memory
- Floppy controller option
- Programmable baud rate

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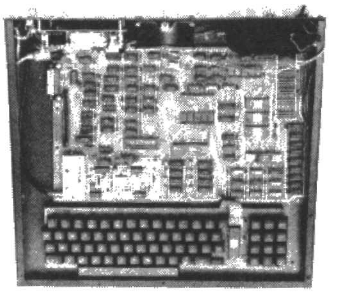

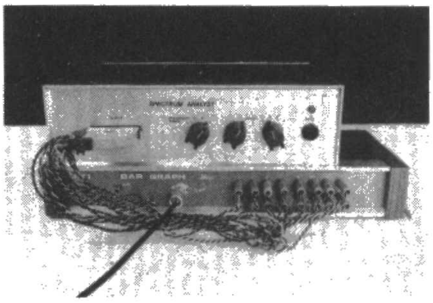

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DIGEST

BREADBOARD 82

Britain's foremost exhibition for the electronics enthusiast, Breadboard, will be springing into life once again this November. Packed with stands from leading firms in the electronics world, the Royal Horticultural Society's New Hall will be turned into the mecca of electronics, but only for a few days (shame!).

Breadboard was first introduced in 1977 as a response to the need for a truly national amateur electronics exhibition. Since that year, it has moved from strength to strength, and the degree of success enjoyed can be gauged by the enthusiasm of imitators trying to get in on the act!

This year will see several innovations, including a Computer Forum, where you'll be able to get 'hands-on' experience of leading micros — this could be very useful if you're contemplating the purchase of a machine yourself. Also on show will be a computer-modulated wargame and visitors to the exhibition will be able to take command of a force in a battlefield simulation. Quite a lot of careful thought has gone into the design of the programs used in these games, so there will be an opportunity to learn about the techniques involved.

Holograms have been around for some years now, and some small examples have even been offered for sale in the pages of ETI, but most people will not have seen the best the medium is capable of. Because the levels of skill and technology involved are very high, there are still comparitively few examples of the state of the art. Breadboard '82 will have a major display of holograms, courtesy of the Light Fantastic gallery, that will include some of the highest quality holograms there are. This will be the fringe show of the year!

In addition there will be daily lectures on topics in the electronics field that cater for all levels of understanding, and competitions, some of which will demand a knowledge of electronics, and some that will test your wits in other fields.

All the Argus Specialist Publications magazines that you know and love will be represented, including your very own ETI, so you can come and meet the people who produce the mags that give you the gen.

BREADBOARD 82 will be at the Royal Horticultural Society's New Hall on the 10th to the 14th November. See next month's ETI for a special eight-page guide to the exhibition.

Small is Beautiful?

Panasonic has launched what they claim is the world's smallest and lightest personal stereo cassette player, complete with featherweight headphones and available in three designs and finishes.

Named the 'Way' Series, these tiny units weigh only 223 grams each (without batteries) and measure 75 mm x 108 mm 28 mm. Their compact dimensions have been made possible by a unique flexible printed circuit board which is only 0.2 mm thick, and can be shaped into a very small space. (Conventional printed circuit boards are about 1 mm thick and inflexible, requiring a larger case).

Panasonic's new tape transport mechanism also contributes to the miniaturisation of the 'Way' Series. Unlike the conventional mechanisms, the head does not change its position in fast-forward and rewind modes, so allowing a very close encasement.

They will be available in the UK from August through the Panasonic network of dealers, at a recommended retail price of £66.50 each, complete with headphones, belt holder, and shoulder strap. For further information contact: National Panasonic (UK) Limited, 300-318 Bath Road, Slough, Berkshire SL1 6JB.

The Last Word in Burglar Alarms?

A new type of sound-activated alarm system is now available in the UK from the Security Systems Division of Elbit Data Systems Ltd of Slough, Berkshire. Called the ELSEC-HARAN, the new system rings your telephone (or several telephones) at any distance when 'intruder' sounds are detected in your premises. By picking up the phone, you can then listen to the sounds being made by any intruders (talking, drilling, opening and shutting drawers, flicking through papers, etc) and take immediate action by using the same telephone to activate sirens, release nerve gas (yes, they really did say that!), lock the thieves in, alert police, or other appropriate countermeasures. Also, you can 'listen in' at any time, or check the system is working, from any telephone anywhere in the world. Further enquiries (though they didn't say they could supply the nerve gas) to: Elbit Data Systems Ltd, Security Systems Division, 295 Aberdeen Avenue, Slough, Berkshire SL1 4HQ. Tel: (0753) 26713.

Computer Warfare

The low-price end of the computer market is beginning to resemble Chicago in the 1930s; friendly competition is out and open 'gang warfare' is in with a vengeance. Clive Sinclair made no secret of the fact that he launched the ZX Spectrum in a fit of pique because the BBC didn't choose him to design their micro; now Oric Products are out gunning for Uncle Clive with thinly disguised zeal. Oric is a new company born out of Tandata Marketing and Tangerine Computer Systems; indeed, the chief designer is Paul Johnson of Microtan 65 and Tantel fame. Their new micro is called the Oric I and the press release about it is subtly scathing about Sinclair. Some typical quotes: "Emphasis has been placed on 'real' computing, the keyboard has 57 moving keys . . .", ". . . no keys have more than two functions", "The Oric I has a dedicated sound generator chip with a real loudspeaker . . .", "Tangerine are the only UK computer company to design their own ULA from scratch. Other manufacturers have the ULA made for them to the specifications of the computer rather than designing the ULA and building the computer round it. This is why the likes of Acorn and Sinclair have so much trouble with ULAs . . .". OK, on second thoughts it's not subtle.

Oric I is to be launched in mid-October and comes in two versions. One has 16K of RAM and costs £99 including VAT, the other has 48K of RAM and costs £169. Both have 16 colours, Microsoft BASIC, teletext/viewdata compatibility, 40 x 24 display, Centronics printer interface and tape cassette ports. Custom printers, modems and disc drives will be available shortly after the launch, and Oric expect sales to reach 50,000+ in the first year. Watch this space for a review (Oric please note). . .

Incidentally, if the name of the computer sounds similar to a certain fictional device, this is probably because Paul Johnson is a confirmed 'Blake's Seven' addict.

Hitachi Hit Back

Hitachi have announced plans to formally enter the UK microcomputer market with the establishment of a new division — Hitachi Computer Products. They will be bringing into the UK a total range of microcomputer equipment, designed, developed, manufactured and marketed by Hitachi, giving a total production strength virtually unmatched in the microcomputing industry. Spearheading Hitachi's penetration of the UK market will be its 16-bit microcomputer, due to make its first public appearance at the NCC in Houston in a few days time. Until now a closely guarded secret, Hitachi Computer Products have been able to reveal some of the major features of the system.

The microcomputer will be a 16-bit machine, selling at under £3,000. It will be comparable to the much heralded IBM personal computer and will be aimed primarily at the business user, though they expect it also to make a good showing in the personal computer market. The base system configuration includes a 64 K byte CPU, detachable keyboard, floppy disk storage, a 16-colour high-resolution CRT display and printer. The system will feature high speed processing, based on the Intel 8088 chip. User RAM is expandable and there is a range of built-in interfaces. The operating system will be MS DOS and available languages include a BASIC interpreter, BASIC compiler, Fortran, COBOL, Pascal and Assembler.

The precise date of the new system onto the UK market has yet to be finalised, but Hitachi Computer Products stresses it will not be made available until a good range of applications software has been developed.

Brochure from Zilog

Zilog have published a brochure that provides comprehensive information on their complete Z8000 family of 16-bit microprocessors, peripherals and support systems. Known as the 'Z8000 Family Technical Overview', it is available free-of-charge to designers and engineers currently engaged in the design and development of 16-bit microcomputer based systems.

The 52 page booklet provides readers with an introduction to the Z8000 family design concept and gives a brief description of Zilog's Z-Bus and how to interface to it. Data sheets of all currently available chips, software and support systems within the Z8000 family are included. Zilog (UK) Limited, Moorbridge Road, Maidenhead, Berkshire SL6 8PL. Tel: (0628) 39200.

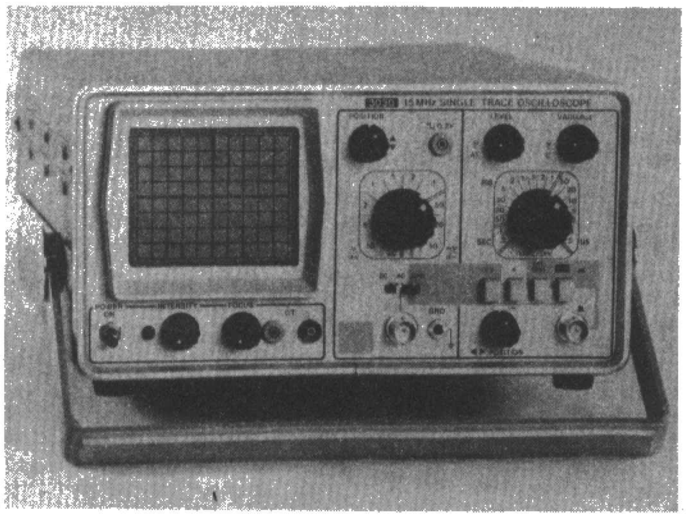
Spectrum Surgery

Here's a story about everyday fault-finding folk that we hope will be of help to someone, somewhere. One of our project editors, Phil Walker, was trying to get the ZX Spectrum to do something — anything at all, in fact, but it persisted in playing dead. Eventually the trouble was tracked down to the power supply, or rather the lack of it. Applying his trained ear to the offending black box, he found no hum or buzz as one might expect, so it was time for surgery. Once inside, all looked well but there was still no action. While poking around for a while with a blunt instrument (no mains present, of course), he happened to prod a small component half-hidden under the transformer. Honest guv, it came away in his hand. The swift application of the workshop soldering iron solved the problem and the trouble appeared to be that the leads of the mains fuse hadn't been inserted into the board far enough before flow soldering. The result was a nice-looking board but no volts.

New Opto-Coupler

A new high reliability opto-coupler giving four channels of opto-coupling capability in a small package is now available from Norbain Electro-Optics Limited.

The output current for each channel is 40 mA at maximum with an output voltage of −0V5 to +20 V within an operational temperature range of −55°C to +100°C. The peak input current per channel is 20 mA with a reverse input voltage of 5 V. Norbain Electro-Optics Limited, Norbain House, Boulton Road, Reading, Berkshire RG2 0LT. Tel: (0734) 864411.



Scope With More Scope

The capabilities of the low cost Type 3030 single trace oscilloscope from Electronic Hobbies Ltd are extended beyond the range of a normal scope with the inclusion of a built-in component tester; active and passive components, including diodes, transistors and FETs can be tested in and out of circuit, test results being displayed instantly on the CRT. Thus the 3030 has increased use as a test and trouble shooting instrument. With front panel controls clearly marked and related functions and controls colour linked, the 3030 is designed to achieve the optimum styling size. Having a 15 MHz bandwidth and deflection coefficients from 5 mV to 20 V/div, it is ideal for investigating low level circuits and allows the on-screen measurement of high level signals. Vertical performance is fully complimented by a wide range time base with 18 sweep speeds plus a variable, covering the range 200 nS to 200 mS/div.

With two trigger modes, automatic and level, the 3030 will lock to any repetitive waveform and display a bright base line at all sweep speeds in the absence of an input signal in the auto mode. The level mode features reliable triggering for complex signals. Giving 50 per cent more display area than normally found for this price range and performance bracket, it has an 8 × 10 div rectangular CRT, with bright high definition display. It also has a 200 mV calibration signal. With the increased usage available in the incorporation of a component tester, this scope would be an ideal test and measuring instrument for any hobbyist or experimenter. Priced at £145 (plus P&P at £12.00 and VAT), the scope is available mail order from Electronic Hobbies Ltd., 17 Roxwell Road, Chelmsford, Essex CM1 2LY.

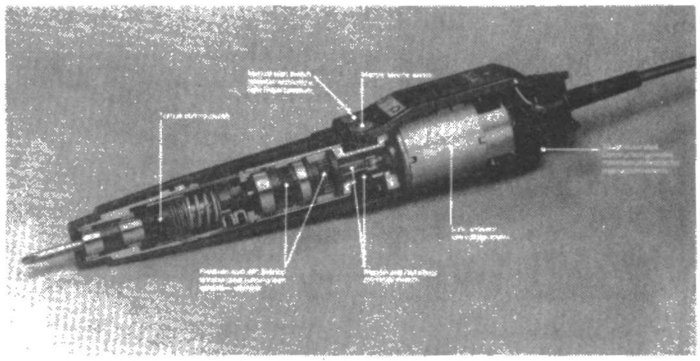
Shorts

- Wilmslow Audio have a new catalogue, and it's as packed as ever with goodies. The cost is £1.50 including post, and it's available from Wilmslow Audio Ltd, 35/39 Church Street, Wilmslow, Cheshire SK9 1AS.
- The press release for the Buck Rogers Burger Station ('Burger Blast Off, Digest 9 January this year) must have fallen through a time-warp, because according to our extra-Galactic sources, the joint has only just opened, at 37 Queen Street, Glasgow.
- Computer books: Kuma Computers, 11 York Road, Maidenhead, Berks, have just issued a new catalogue; Elkan Electronics, 28 Bury Road, Prestwich, Manchester M25 8LD have just published "101 Pocket Computer Tips & Tricks" by Jim Cole, price £5.95 including p&p, which is aimed at Sharp PC1211 and TRS-80 pocket-computer users.
- Two new lithium power systems for portable calculators are now available in the UK from Rayovac Ltd to supplement the company's existing range of lithium, silver-oxide and mercuric-oxide batteries. These new long-life coin cells are highly leak-resistant and have exceptional shelf life. They are available in five sizes. Rayovac Limited, Station Approach, St Mary Cray, Orpington, Kent BR5 2ND. Tel: (66) 70516.
- A large quantity of JVC E180 tapes were stolen in W. Germany recently, so view any special offer from dubious sources on such tapes with suspicion, and if, as a dealer, you are approached, please contact JVC (UK) Ltd, Eldonwall Trading Estate, Staples Corner, 6–8 Priestley Way, London NW2 7AF.
- Latest addition to the HB Electronics range of highly effective production aids is the lightweight Ungar Desoldering Pump. HB Electronics, Lever Street, Bolton BL3 6BJ. Tel: (0204) 386361.
- The National Wireless Museum is offering free technical information on very old pieces of electronic equipment, copied from their archives. Contact Douglas Byrne (the Curator) on 0982-62513, or write to him at Arlington House, 34 Pelhurst Road, Ryde, Isle of Wight, for a service sheet for Aunt Agatha's pre-war set.
- The BBC is now making available details of all new transmitter openings on page 196 on Ceefax (BBC1).
- A range of Weller de-soldering equipment — including a portable workstation for service applications — is now available through Axiom Electronics Limited, the High Wycombe based distribution house. Axiom Electronics Limited, Turnpike Road, Cressex Estate, High Wycombe, Bucks HP12 3NR.
- If your company uses dot matrix printers for the production of bank giro credits, then you should check that it will be acceptable for high-speed machine reading, as the banks' credit clearing system will be automated at the end of 1983. For full technical details contact: The Inter-Bank Standards Unit, 32 City Road, London EC1Y 1AA.

Hefty Hi-Fi

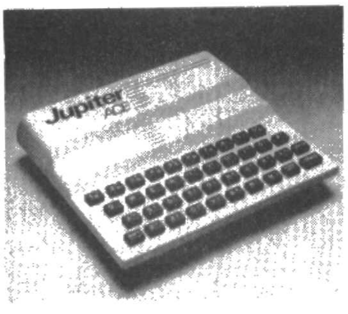
HH Electronic have announced an important new model, the M900, to add to their famous stable of MOSFET power amplifiers. This new amp asserts HH's continuing leadership in the area of amplifiers and offers virtually flawless performance at less cost per watt of output. HH MOSFET technology offers the power amp user the following benefits: exceptional reliability under tough load conditions from well-proven HH MOSFET devices; high accuracy response and cleaner sounds by state-of-the-art circuit design; excellent stability from the moment of switch-on as a benefit of the balanced differential circuit layout; and tremendous output power from a massive 1.2 kVA mains transformer and 30,000uF computer grade electrolytic capacitors. The M900 is packaged in a rugged functional 19" rack-mount casing, ideal for on-the-road sound reinforcement applications and perfect in studio or commercial sound installations. Optional balanced input transformers are available and inputs are set by 'potentiometer locks' which allow the user to fix the gain levels. Professional XLR connectors are features on outputs and inputs, and a large diameter quiet running fan keeps the amp cool even under continuous duty cycle heavy load conditions.

The M900 is available from June 1982 at a very competitive price. For further details contact HH Electronic, Viking Way, Bar Hill, Cambridge CB3 8EL.



Spin Your Screws

A rather nifty bit of hardware is now available for people who've got a lot of screwing to do — the Desoutter electric screwdriver. This is the first British torque-controlled device and comes in two versions at present; an automatic push-start model and a manual start version. The auto screwdriver will begin to operate as soon as light axial pressure is applied to the bit. Once the pre-set torque has been reached the clutch disengages and the motor is switched off at the same time, reducing any inertia that might be transmitted to the screw. The manual start version has start and reverse buttons instead; there is a manual mode on the auto version for situations where this would be convenient. There are a number of accessories available including 90° or 45° angle head attachments and a multi-station supply module which provides 10 individually fused output sockets. The screwdriver is safe in operation as it runs at a low voltage via a mains transformer, and the noise level is less than 60 dBA (that's no louder than normal conversation). Although the screwdrivers are intended for modern precision assembly work in industry, we'd love to have one in our workshop — accountants being what they are we can only dream, though. For more information you can contact Desoutter Ltd at 319 Edgware Road, Colindale, London NW9 6ND.



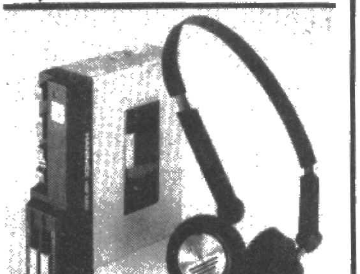
Interesting New Computer

Jupiter Cantab, a British company owned and run by leading computer designers Richard Altwasser and Steven Vickers have announced a new personal computer, the Jupiter Ace, that features full-size moving key keyboard, user-defined high resolution graphics, sound and a revolutionary microcomputer language, Forth. The machine is available only by mail order for an all-inclusive price of £89.95. Orders will be accepted from September onwards.

Hanimex Hardware

Hanimex UK have sent us details of their latest electronic gadgetry which is being launched. Their new video computer TV game (yes, another one!) has a range of cartridges to satisfy any addict of the arcade games such as Defender, Galactica, Pucman (sic), Robot Killers etc etc etc. The machine is expected to retail at £89.95 with the cartridges costing £19.95 each. The blurb says that the colour generation and graphics of the games gives stunning 3D visual effects, 'a feature not previously available on home computer games'. Haven't they seen the new Ataris yet?

The remaining items are in the field of personal hi-fi and include the HSP 2200 personal cassette, the



HDR 1320 portable stereo clock radio with headphones and the HSR 1020 FM stereo radio with headset.

AT THE THIRD STROKE BRITISH TELECOM'S PROFIT WILL BE £458 MILLION PRECISELY . . .

SATELLITE TV

There are giant footprints all over Europe, and they're a helluva lot more than seven leagues apart. It's all part of the system to bring you soap opera from the skies, as Vivian Capel explains.

Somewhat belatedly, the British Government has given the go-ahead for satellite TV in this country, with two BBC stations to start transmitting in 1986 — several years behind countries like America, Russia and India. In fairness it should be added that the service in other countries is either experimental, or a link to transmitters in remote areas, and not yet a full public service.

Originally there was a choice between the European Communications Satellite which carries two channels and the larger L-Sat which carries five. Five channels have been allocated by the International Communications Union to each country, so with two already assigned to the BBC plus narrower bandwidth radio services, and the IBA showing interest, it is virtually certain that L-Sat will be chosen.

L-Sat stands some 18 ft high, equivalent to two storeys of a house, and 13 ft wide. From the sides sprout two enormous 'wings' which carry the large number of solar panels required to power the transmitters and ancilliary equipment. Each channel will transmit some 200 W of RF in the case of the UK satellite, though other countries' satellites requiring wider area coverage will need higher powers and smaller countries will get by on lower powers. So 1,000 W or more in total will be radiated from the five channels, and with an efficiency of about a third, this means the power requirement will be over 3,000 W. The receiver for the 'up' link and various other items bring the total up to 4 kW, although a higher power capability is planned for future models.

The Back-Up

In this project, 'spares' mean spare *satellites* complete with all mod cons. To avoid protracted loss of service should a fault occur, a second satellite must always be in orbit as a back-up. So, the investment needed is doubled, but it does not end there. Should a fault appear and the back-up satellite be put into service, there is no further back-up should that one fail. Hence, a third satellite must be ready on earth for quick launch to take over as a back-up. This brings the estimated cost up to around £150 million for each satellite and associated back-up.

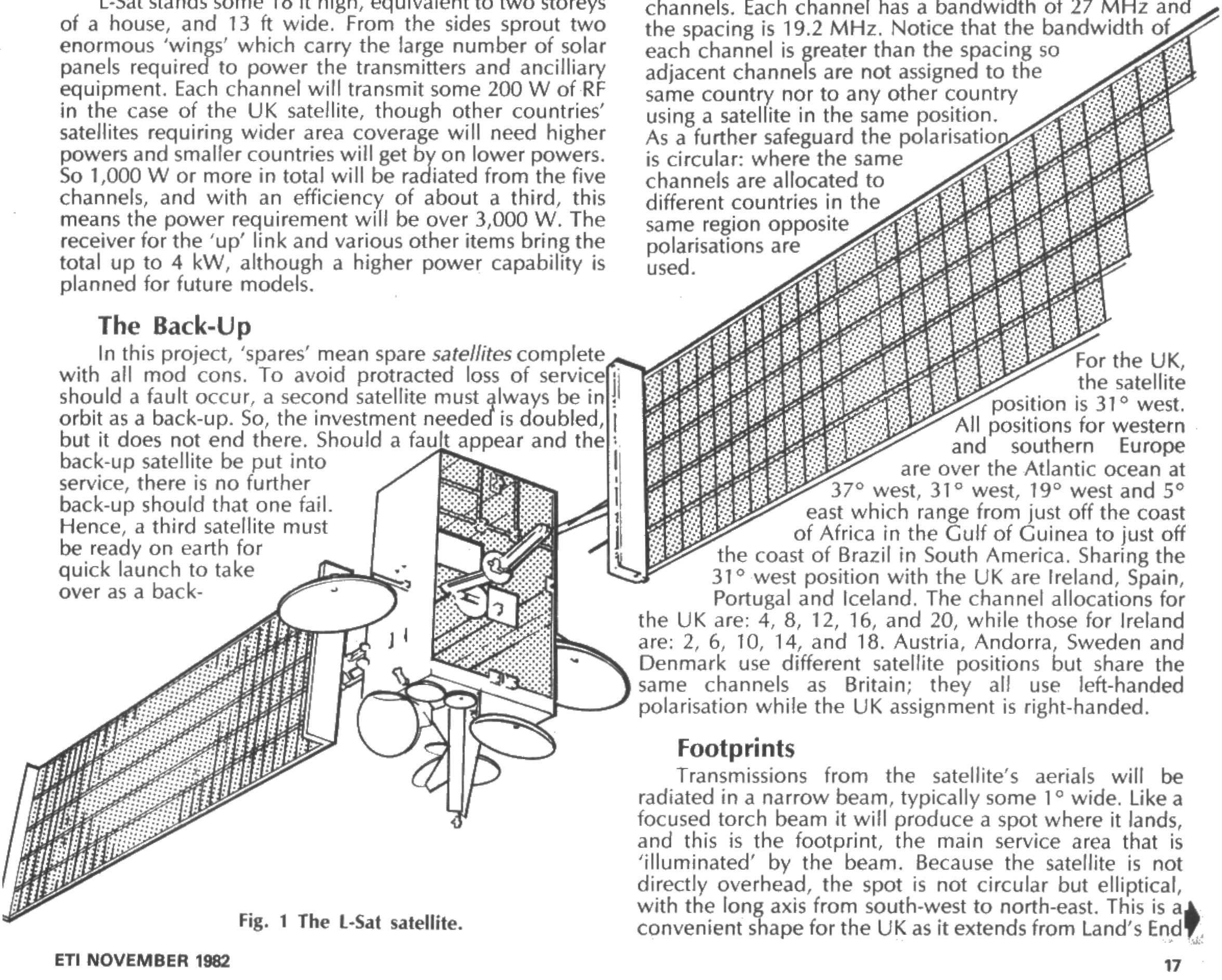


Fig. 1 The L-Sat satellite.

International Allocations

The International Telecommunications Union met in Geneva in 1977 to allocate positions and frequencies for future use by participating countries. Positions were established around the equator at 6° intervals and these were assigned to countries most suitable for their geographical location. Some countries with common interests received the same positions so that recipients could pick up transmissions from the other satellites without users re-aiming their aerials.

The frequency band to be used is 11.7-12.5 GHz (a gigahertz is 1,000 MHz), which is divided into 40 channels. Each channel has a bandwidth of 27 MHz and the spacing is 19.2 MHz. Notice that the bandwidth of each channel is greater than the spacing so adjacent channels are not assigned to the same country nor to any other country using a satellite in the same position. As a further safeguard the polarisation is circular: where the same channels are allocated to different countries in the same region opposite polarisations are used.

For the UK, the satellite position is 31° west. All positions for western and southern Europe are over the Atlantic ocean at 37° west, 31° west, 19° west and 5° east which range from just off the coast of Africa in the Gulf of Guinea to just off the coast of Brazil in South America. Sharing the 31° west position with the UK are Ireland, Spain, Portugal and Iceland. The channel allocations for the UK are: 4, 8, 12, 16, and 20, while those for Ireland are: 2, 6, 10, 14, and 18. Austria, Andorra, Sweden and Denmark use different satellite positions but share the same channels as Britain; they all use left-handed polarisation while the UK assignment is right-handed.

Footprints

Transmissions from the satellite's aerials will be radiated in a narrow beam, typically some 1° wide. Like a focused torch beam it will produce a spot where it lands, and this is the footprint, the main service area that is 'illuminated' by the beam. Because the satellite is not directly overhead, the spot is not circular but elliptical, with the long axis from south-west to north-east. This is a convenient shape for the UK as it extends from Land's End ➧

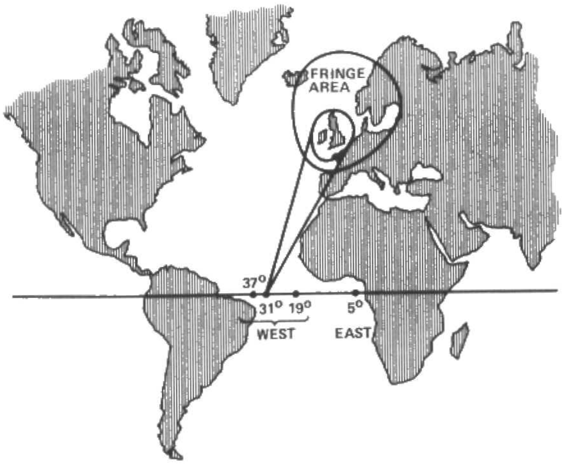


Fig. 2 The footprint from the UK satellite, with its fringe area, and the three other positions for Western European satellites.

right up to the Shetland Islands, and from west to east embraces most of Ireland across to northern France. Actually the beam shape, and hence that of the footprint, can be modified by specially designing the aerial reflector; this will be necessary for some countries.

Within the service area, a signal strength of 140 uV/m is anticipated, and this will provide a good signal to the receiver from an aerial with a dish of 1 metre diameter. As with a torch team, there is illumination of reduced intensity beyond the main spot; a fringe area which will cover most of western Europe and Scandinavia with a signal strength (on average) about 8 dB less than that of the main service area. To receive this satisfactorily a reflector of 2 metres would be required. This larger footprint is not an ellipse because the curvature of the earth becomes increasingly important as the beam spreads northward. The shape is more like an inverted pear.

It follows that fringe area reception from mainland European satellites will be possible in Britain. There are some enthusiastic experimenters who already receive Russian transmissions from the Gorizont satellite by using large dishes and conversion equipment. This satellite is not a public service one, but serves as a link between studios and distant transmitters. It radiates at 4 GHz and so would not be receivable with equipment designed for the coming 12 GHz satellites.

Tracking Your Quarry

Foreign-programme hunters will need to look at the footprints of their quarry to see if worth-while signals can be picked up. Generally, the closer they are the stronger will be the fringe area signal. They will also need to know the position of the satellite so as to aim the receiving dish in the right direction.

While all satellite transmissions will be frequency-modulated and within the specified channels, it is to be expected that the actual video and sound signals will in most cases conform to the standards already used by the respective countries for their existing terrestial transmissions. If this were not the case, existing receivers would be rendered obsolete, or unable to receive the the additional services without elaborate converters.

On this assumption, receiving the programmes of other countries from their satellites will depend on whether their existing TV standards are compatible with those of the UK. As may be expected, standards differ, but in most cases are close enough to make reasonable reception possible with a receiver equipped to pick up the UK satellite transmission.

For a start, all European systems employ 625 lines and 50 fields-per-second (except for the high-definition 819-line monochrome French service; but they also run a 625-line colour transmission).

Channel width is 7 MHz for VHF radiation, and 8 MHz for UHF. A number of countries have transmissions on both VHF and UHF, as has Britain, but it is likely that VHF will be phased out as it will be here, so only the UHF transmission standard will remain. Vision bandwidth is in most cases the same at 5 MHz. The spacing between vision and sound carriers is 6 MHz for the UK, but 5.5 MHz for most of the other countries. This would give a slight deterioration of the picture when tuning for optimum sound. Vision modulation is negative in most cases and the sound carrier is frequency modulated.

Furthermore, most of the western European TV systems use the PAL colour coding. The odd ones out are France, Monaco and Luxemburg which have adopted SECAM. These have further differences in that they use positive modulation of the vision signal and the sound signal is amplitude-modulated. They are thus quite incompatible without special modification to the receiver.

Most of the countries of eastern Europe as well as

TABLE 1

COUNTRY	CHANNELS	LATITUDE	POLARISATION	PRESENT SYSTEM	
Monaco	21, 25, 29, 33, 37	37°W	RH	SECAM	C, G, L
Andorra	4, 8, 12, 16, 20	37°W	LH	PAL	B
Ireland	2, 6, 10, 14, 18	31°W	RH	PAL	I
UK	4, 8, 12, 16, 20	31°W	RH	PAL	I
Portugal	3, 7, 11, 15, 19	31°W	LH	PAL	B, G
Iceland	21, 25, 29, 33, 37	31°W	LH	PAL	B
Spain	23, 27, 31, 35, 39	31°W	LH	PAL	B, G
France	1, 5, 9, 13, 17	19°W	RH	SECAM	L, E
Luxemburg	3, 7, 11, 15, 19	19°W	RH	SECAM PAL	L G
Belgium	21, 25, 29, 33, 37	19°W	RH	PAL	B
Netherlands	23, 27, 31, 35, 39	19°W	RH	PAL	B, G
West Germany	2, 6, 10, 14, 18	19°W	LH	PAL	B, G
Switzerland	22, 26, 30, 34, 38	19°W	LH	PAL	B, G
Italy	24, 28, 32, 36, 40	19°W	LH	PAL	B, G
Turkey	1, 5, 9, 13, 17	5°E	RH	PAL	B, G
Greece	3, 7, 11, 15, 19	5°E	RH	SECAM	B, G
Cyprus	21, 25, 29, 33, 37	5°E	RH	PAL	B, G
Iceland					
Azores	23, 27, 31, 35, 39	5°E	RH	PAL	B
Greenland					
Finland	2, 6, 10, 22, 26	5°E	LH	PAL	B, G
Norway	14, 18, 28, 32, 34	5°E	LH	PAL	B, G
Sweden	4, 8, 30, 34, 40	5°E	LH	PAL	B, G
Denmark	12, 16, 20, 24, 36	5°E	LH	PAL	B

TABLE 2

SYSTEM	LINES	FIELDS	CHANNEL WIDTH (MHz)	VISION BANDWIDTH (MHz)	VISION/SOUND SEPARATION (MHz)	VISION MODULATION	SOUND MODULATION
B	625	50	7	5	5.5	NEG	FM
C	625	50	7	5	5.5	POS	AM
E	819	50	14	10	11.15	POS	AM
G	625	50	8	5	5.5	NEG	FM
I	625	50	8	5.5	6	NEG	FM
L	625	50	8	6	6.5	POS	AM

Russia use SECAM colour encoding, but their vision signal is negative and the sound carrier frequency-modulated. Hence they could be received in black-and-white without modification to the receiver. Having more distant footprints, greater sensitivity would be required which would mean a large dish, of at least 3 metres.

Table 1 gives some Western Europe satellite allocations with present TV systems, while Table 2 lists the details of the current TV systems.

Better TV?

With a satellite channel bandwidth of 27 MHz, it is possible to opt for high definition TV, using more lines and better definition along each line. Larger screen TVs show up the deficiencies in our present transmissions all too clearly — this is one of the reasons why projector TVs have not progressed beyond being novelties. Better definition may lead to larger pictures — but it doesn't mean that the programmes will necessarily be any better!

Reception

To achieve the specified signal strength the dish must be very accurately aimed at the satellite. Accuracy should be within 0.1°, which is an exceedingly narrow angle. This must be achieved both horizontally and vertically. It can be seen that far more precision will be required than presently needed for aiming UHF TV aerials. Anyone who has tried to pick up a particular star with a telescope knows how difficult it is to get an accurate fix. And, of course, the satellite will not be visible.

Figure 3 shows the positions of earth and satellite to scale so some idea of the distance out can be obtained. Beam extremities are shown at latitudes 50° (Land's End) and 60°, which bisects the Shetlands. Horizons are drawn for both these latitudes, and the satellite elevation above the horizon will be 34° for Land's End and 22° for the Shetlands. Most of the country will therefore fall between these two.

The satellite position will be quite low, especially in the north, and so shielding by mountains, large buildings or other obstructions to the south-west may render the signal unobtainable. As in difficult areas with the present terrestial services, communal aerials and distribution systems may have to be employed. While the satellite elevation even in the north is greater than that of any distant land-based mast, the much higher frequencies are less prone to diffract around obstacles, and propagation and reception is only possible in line-of-sight positions.

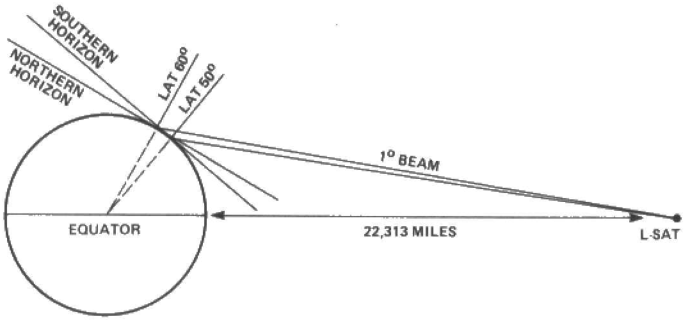


Fig. 3 Scale diagram of the satellite position with beam spread from latitude 50° to 60° (Land's End to Shetlands). The elevation is above the horizon is 34° (at latitude 50°) and 22° (at latitude 60°).

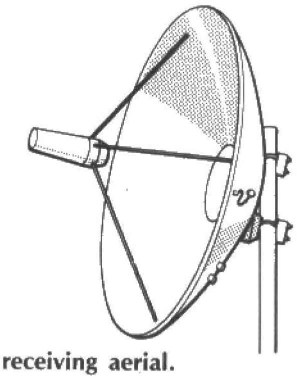


Fig. 4 A typical receiving aerial.

Precision alignment will undoubtedly call for the use of special instruments. A problem will exist for anyone wishing to sample the programmes from other satellites as this will mean re-aiming the reflector. Providing the dish is accessible, a mounting with pre-set adjustable click-positions may be the answer. Alternatively two or more dishes could be installed permanently aligned to other positions, though this would be rather expensive.

Dishy Aerials?

With such a narrow acceptance angle, the effect of wind could be serious, causing fluttering and fading. Snow and ice would change the shape of the reflector and reduce the signal brought to focus, so the dish will have to be weather-proofed in some way, and this will probably mean total enclosure. Who knows, a whole industry may grow up to provide suitable covers that also fit in with the surrounding roof — because the aerials are going to be a good deal larger and more obtrusive than the UHF aerials we presently use.

Apart from the reflector aerial, circuitry will be needed to distinguish between left and right-hand polarisation, and also a frequency-converter to step the frequency down to the UHF band suitable for standard TV receivers. Even low-loss coax would have a very high attenuation at 12 GHz, so the converter would have to be mounted with the aerial unless waveguides were used for the downlead.

A further requirement at the receiver end would be an FM/AM converter as the satellite signal is frequency-modulated. Receivers produced when the satellites become operational will very likely be dual-standard, capable of receiving both FM and AM signals. This will eliminate the last item, but the other circuitry mentioned above will still be required.

It can be seen from this that the £200 figure recently quoted for the necessary equipment to receive satellite TV and which has been challenged as too high, is probably quite near the mark, especially allowing for inflation over the next four years. **ETI**

16 BIT COMPUTER

Announcing the ETI Cortex, in all its 16-bit splendour. This advanced design uses up-to-the-minute technology and forms the basis of a powerful home or business system.

Setting records is getting to be a habit at ETI. We were the first magazine to publish a DIY computer project (the System 68) and we were the first magazine to publish a one-board home computer (the Triton). Now we're the first magazine to publish a full-feature 16-bit computer, and at a price that makes a lot of commercial machines look a bit sick. The Cortex forms the basis of a versatile computer system that expands with your imagination and is based on state-of-the-art VLSI technology; the 'why use five chips if one will do?' philosophy.

Processing Power

The processor is a high-speed 16-bit device which possesses a unique system of RAM-based registers. The Cortex kit is supplied with a full 64K bytes of dynamic RAM (ie 32K words of 16 bits), and 24K of BASIC and assembler in an overlaid memory organisation (we'll explain what that means later). The high definition colour VDU has a separate 16K of RAM outside the CPU's 64K memory map and some extraordinary features that result in superb graphics capabilities. Disc drives may be interfaced easily as the controller chips fit on the PCB, and the resident BASIC can be overwritten by disc-based languages; the first that will be available is UCSD Pascal. The latter features will make the system particularly attractive to business users, and Cortexes (Corti?) will be available ready-built as well as in kit form.

Incidentally, we made a slip of the typewriter last month. What we meant to say was *"Chips* designed by Texas Instruments . . ." Sorry for any confusion caused.

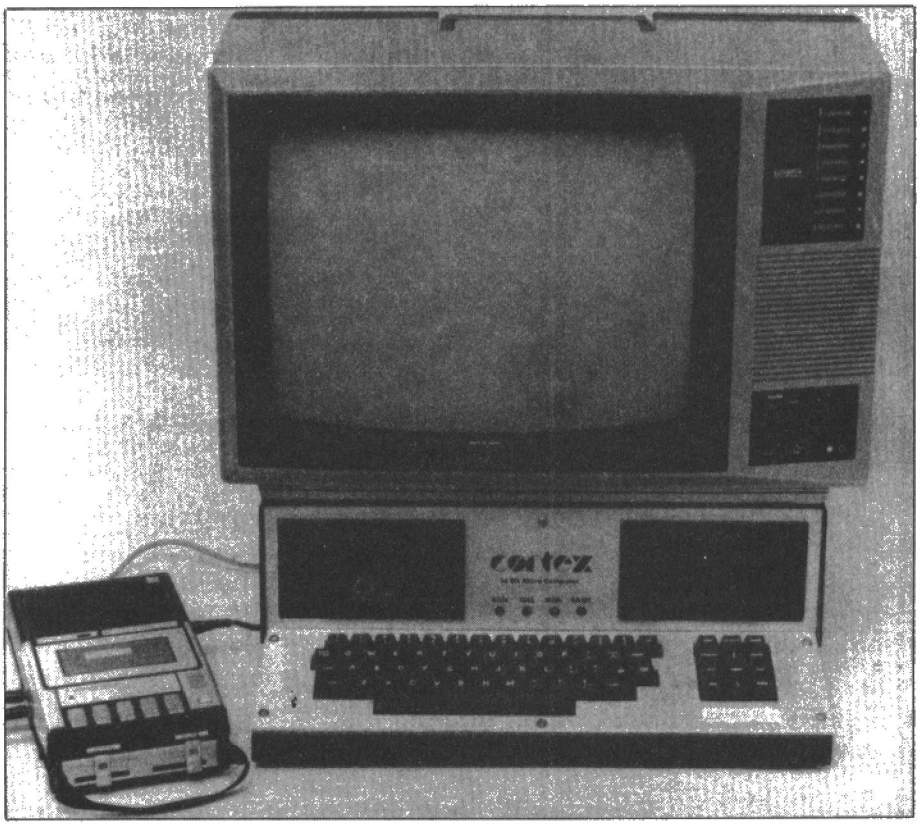
The heart of the Cortex is the TMS9995 CPU. As with all the components in this project it was selected from the wide range of currently available CPUs on a price/performance basis. The 9995 is based on the unique memory-to-memory architecture of the TMS9900. Thus it has the same architectural features of this powerful 16-bit processor and an enhancement of its rich, mini-computer style, instruction set. It is fabricated in state-of-the-art N-channel silicon gate MOS technology, enabling single 5V operation and high speed (12MHz) to be achieved in a compact silicon area.

As well as the 16-bit CPU, fabricated onto the same chip are a number of extra features that make this device the obvious choice for a large number of general purpose applications. 256 bytes (128 words) of on-chip RAM enables four complete, fast access register files (workspaces) to be implemented in full speed memory. A clock generator is also included to minimise the number of external components. Also available are a timer/event counter, a prioritised Interrupt Interface and a 16-bit flag register which can be output on the I/O control bus. The I/O bus is completely separate from the main memory map, and enables 32K of individual I/O bits to be manipulated individually or simultaneously in groups.

Artful Architecture

The term 'memory-to-memory' implies the fundamental difference between traditional eight-bit CPU architectures and that of the 9995. That is, all transfers in the machine are from one main memory location to another. Only three 16-bit registers exist on the CPU itself; the Program Counter, the Status Register and the Workspace Pointer.

The Workspace Pointer contains the address of the start of a block of RAM anywhere in the main memory map. This address is designated register zero; the next 15 contiguous memory locations are designated Registers 1–15. These registers may then be used by the



A complete Cortex system.

programmer as scratch registers. A large number of instructions exist that make maximum use of the reduced addressing needed to access these. For example MPY R4, R5, performs a 16-bit multiply of the contents of Register 4 with Register 5 and stores the 32-bit result in Register 5 (most significant word) and Register 6.

What advantage does this give a programmer over other architectures? Well, in addition to providing no restriction on the choice of addressing modes (register 0 can still be accessed as memory location 7XXXX) the power comes when an interrupt or other subroutine call occurs. It is obviously desirable, especially on receipt of an interrupt, to be able to react as rapidly as possible. On a register-oriented machine it is necessary to save the contents of the working registers in main memory, a slow operation requiring a large number of reads and writes to push the registers onto the stack. On the 9995 the context switch occurs by changing the value in the Workspace Pointer. This points to a new area of fresh registers ready to process the interrupt. The full context of the previous operation is retained in the previous workspace registers, which, being in main memory, are still preserved intact. A return is similarly implemented easily and rapidly by restoring the old Workspace Pointer value. In many real time control situations with a large number of external events occurring this architecture is the only one that allows for efficient processing.

External Affairs

The system clock is externally generated and fed to the CPU via the XTAL2 input. A clockout signal is also provided that is one-fourth of the crystal frequency (3 MHz). The 64K bytes of system memory are directly addressed by A0-A15. Here the convention is that A0 is the most significant bit. A0-A14 are also used to directly address the separate I/O structure of the Communication Register Unit (CRU). The bit to be accessed is held on A0-A14 and the data is present on A15. The data is then clocked out by $\overline{\text{CRUCLK}}$. Reading a CRU bit into the CPU is achieved in the same manner but is read into the CRUIN line.

The data bus is multiplexed from the internal 16-bit architecture to eight bits externally, D0-D7. A memory access is signalled by $\overline{\text{MEMEN}}$ and data direction is controlled by $\overline{\text{DBIN}}$. $\overline{\text{WE}}$ indicates a memory write. For the control of slow memories a READY line signals to the CPU if the memory is ready to complete the current access. If not, the CPU waits for another CLKOUT cycle before continuing.

In the Cortex all these features are used to provide the fastest BASIC available to a home constructor. Even then the speed is still limited by I/O transfers. This can be seen as evidenced by the amount of time the 'idle' LED is on. This LED is directly driven by a status decoder that indicates when the CPU is no longer executing any instructions but is waiting for an external interrupt.

Dynamic Designing

We don't doubt that all you digital dabblers have watched the plummeting price of memory in our advertisers' pages, and the most dramatic trend has been in dynamic memory (DRAM). This is partly due to the simplicity of the basic cell design in a DRAM; and this simplicity means in turn that the most dramatic cell density increases have been and will be made in DRAMs. With 16K DRAMs prices have pretty much levelled out at the bottom of the curve, but the 64K DRAMs are in hot pursuit.

More importantly from the technical point of view, certain 64K DRAMs offer upward compatibility to the next generation of 256K DRAMs. (Why are the steps quadrupling: 16K to 64K to 256K? Because DRAMs have a two-part

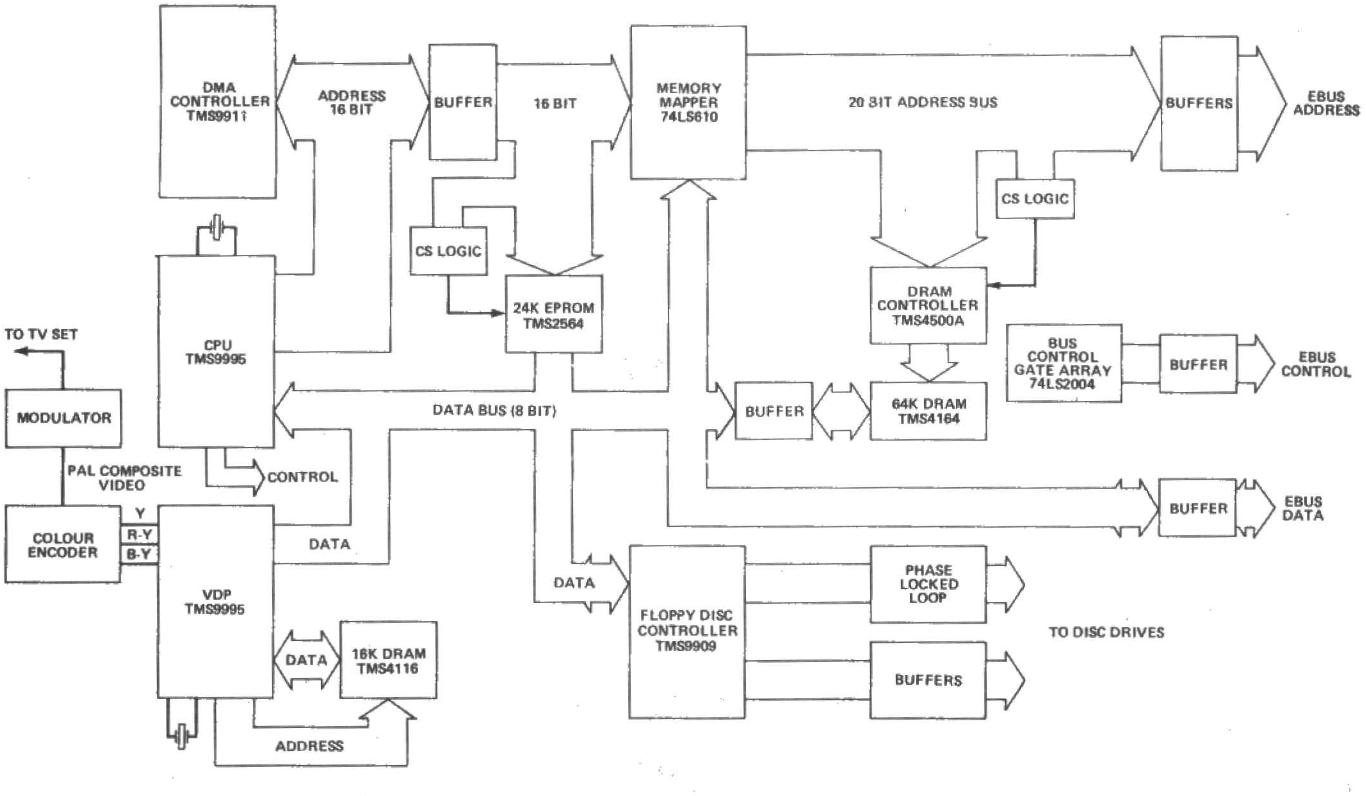


Fig. 1 Block diagram for the complete Cortex.

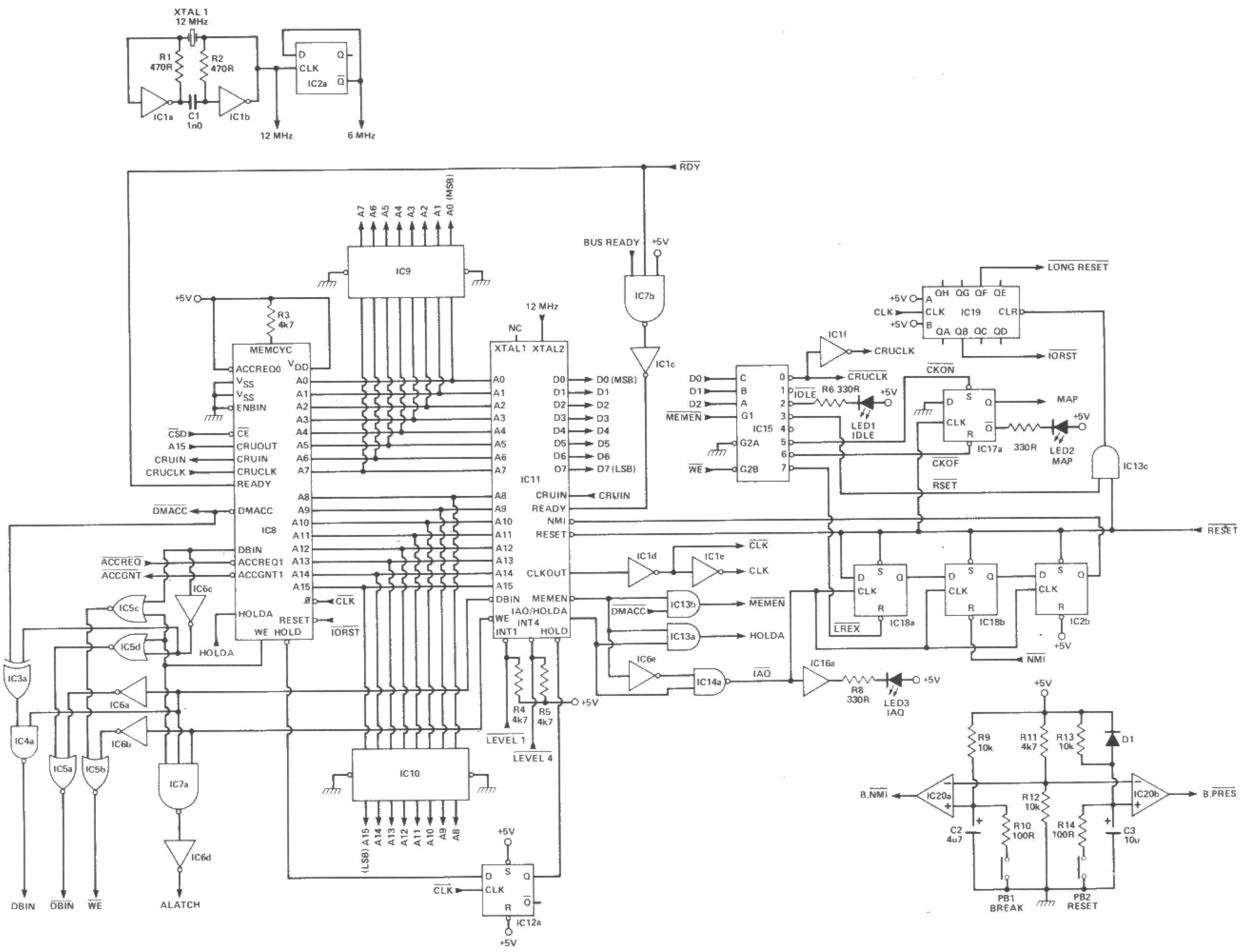


Fig. 2 Circuit diagram of the CPU and DMAC circuitry.

HOW IT WORKS — CPU AND DMAC

The heart of the system is the CPU, IC11 (a TMS9995). It has a 16-bit internal architecture and an eight-bit wide external data path. The master clock for the system is formed by IC1a,b and associated components; the 12 Mhz clock rate of the CPU enables it to complete a memory read or write in only 166 nS! This is too fast for present DRAM technology so the automatic wait state feature of the CPU is used. This automatically assumes that memory is not ready and extends the memory access to 500 nS. The cycle can be further extended by a low level on the READY input to the CPU; this occurs, for example, when the DRAM is not ready because a refresh cycle is taking place.

The CPU signals the type of memory cycle by driving either DBIN or WE (write) low after driving MEMEN low. If the memory cycle is an instruction fetch then the IAQ/HOLDA signal goes high until both bytes have been fetched. This condition is decoded by IC6e, IC14a and buffered by IC16a to light LED3 to provide a front panel indication.

The CPU has a bit-mapped I/O interface which is separate from the memory data bus; the process is carried out by a section of the CPU called the Communications Register Unit (CRU). The data transfers are serial, bit by bit, each bit having a unique address. This allows 32K bits to be accessed (not 64K since address line A15 carries the data). The value of the data bit is on CRUOUT (A15) for output cycles and a WE/CRUCLK pulse is generated to strobe the data into the I/O devices. On input cycles the data is sampled from the CRUIN line and a pulse is generated on the DBIN line to enable the bus buffers and so on. During all serial I/O operations the MEMEN signal stays high. Any number of bits from one to 16 can be transferred, each bit taking 500 nS to transfer if the READY input is high.

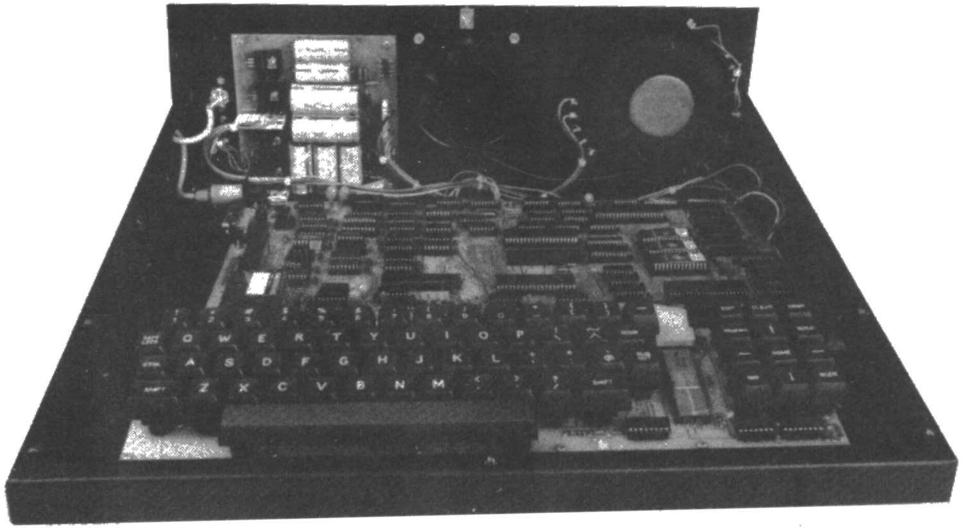
There are some special I/O signals for control use called IDLE, LREX, CKON, CKOF and RSET. IC15 decodes these separately from the normal I/O operations by using the three-bit code output on D0–D2 of the data bus. IDLE pulses continuously whenever the IDLE instruction is executed; it indicates that the CPU is in an internal loop waiting for interrupts (ie doing nothing). LED1 on the front panel lights to indicate this state. LREX is used for the single instruction execution logic which causes an NMI interrupt to occur two instructions after executing the LREX instruction. The two-instruction delay is generated by the series flip-flops IC18a, IC18b and IC2b.

CKON and CKOF are used to switch the memory mapper device from passive to active and vice versa: the signals set or reset the Q output of IC17a to enable or disable the memory mapper (IC26) via IC24a, 25a. When Q is high, Q is low, and LED2 lights to signal that external memory is being accessed.

The RSET signal causes all I/O devices to be reset and sets the CPU interrupt mask to disable all interrupts. Normally both RESET and RSET are high, so the output of IC13c is high and IC19, an eight-bit parallel-out serial shift register, clocks out a continuous series of 1s. A low on RSET or RESET sets all the outputs of IC19 low (specifically IORST and LONG RESET); when the CLR input returns high, 1s are clocked through the shift register first taking IORST then LONG RESET high.

The Direct Memory Access controller (IC8, a TMS9911) is used to provide transparent high speed data transfer to and from the floppy disc controller (FDC) into memory. The address bus of the CPU is tri-state, as are the address outputs of the DMAC. Only one device is in control of the address bus at any one time. When the FDC requires the memory it signals on ACCREQ (access request); the DMAC then signals to the CPU using the HOLD signal that it requires the bus. When the CPU reaches the end of the current memory cycle it tri-states all its outputs (except MEMEN) and signals HOLDA ('acknowledged'). The DMAC now takes over the bus, signals ACCGNT to the FDC, and transfers the data byte between the memory and the FDC.

After completing the memory cycle(s) the DMAC then relinquishes control back to the CPU by releasing HOLD. The CPU then continues as if nothing had happened. The TMS9911 was designed for use with the TMS9900 CPU; when it is used with the TMS9995, extra gating is required to make the signals compatible. Parts of ICs 3, 4, 5, 6 and 7 take care of this. In this application only one of two channels in the DMAC is used; the other is free for the user to experiment with.



multiplexed address bus, so adding one extra address pin is the equivalent of two extra address lines and thus four times the addressing range.) Since all 16K DRAMs operated on a 128-cycle refresh, some 64Ks followed suit. However, that extra address pin called for twice the number of sense amplifiers on the chip, which occupied valuable silicon area (see this month's article on Designing Micro Systems for more about DRAM structure). For 256K DRAMs the waste of chip area is intolerable and to get a product that is capable of manufacture, 256-cycle refresh is essential. The TMS4164 64K DRAM, the first commercially available production device, adopted 256-cycle refresh from the start, as well as following the JEDEC-approved pin-out. This means that the devices are not only upward pin-compatible from the TMS4116, but will also be upward compatible in the future to 256K devices. Simply plug new chips in the old sockets and you've got four times the memory!

For these reasons we chose the TMS4164 to provide a full 64K memory map using only eight chips. Not only is it compact, fast and very reliable, but it is the first 64K device to be successfully encapsulated in a low-cost plastic package.

In our application, refresh is achieved in a manner typical of the Cortex philosophy; a single-chip DRAM refresh controller is used, the TMS4500A. This device provides all the necessary control and arbitration functions for handling 64K DRAMs in a microprocessor system. It accepts the 16 address lines, A0–15, and multiplexes them to row address and column address (RAS and CAS) at the appropriate times, generates refresh signals for 128 or 256-cycle memories and arbitrates synchronously between access requests and refresh cycles. Synchronisation is important for achieving reliable arbitration, and the CPU clock is utilised as the main timing reference.

ROM To Manoeuvre

Similar design criteria were applied to the choice of EPROMs to store the system firmware. In order to economically store the large number of bytes required to provide

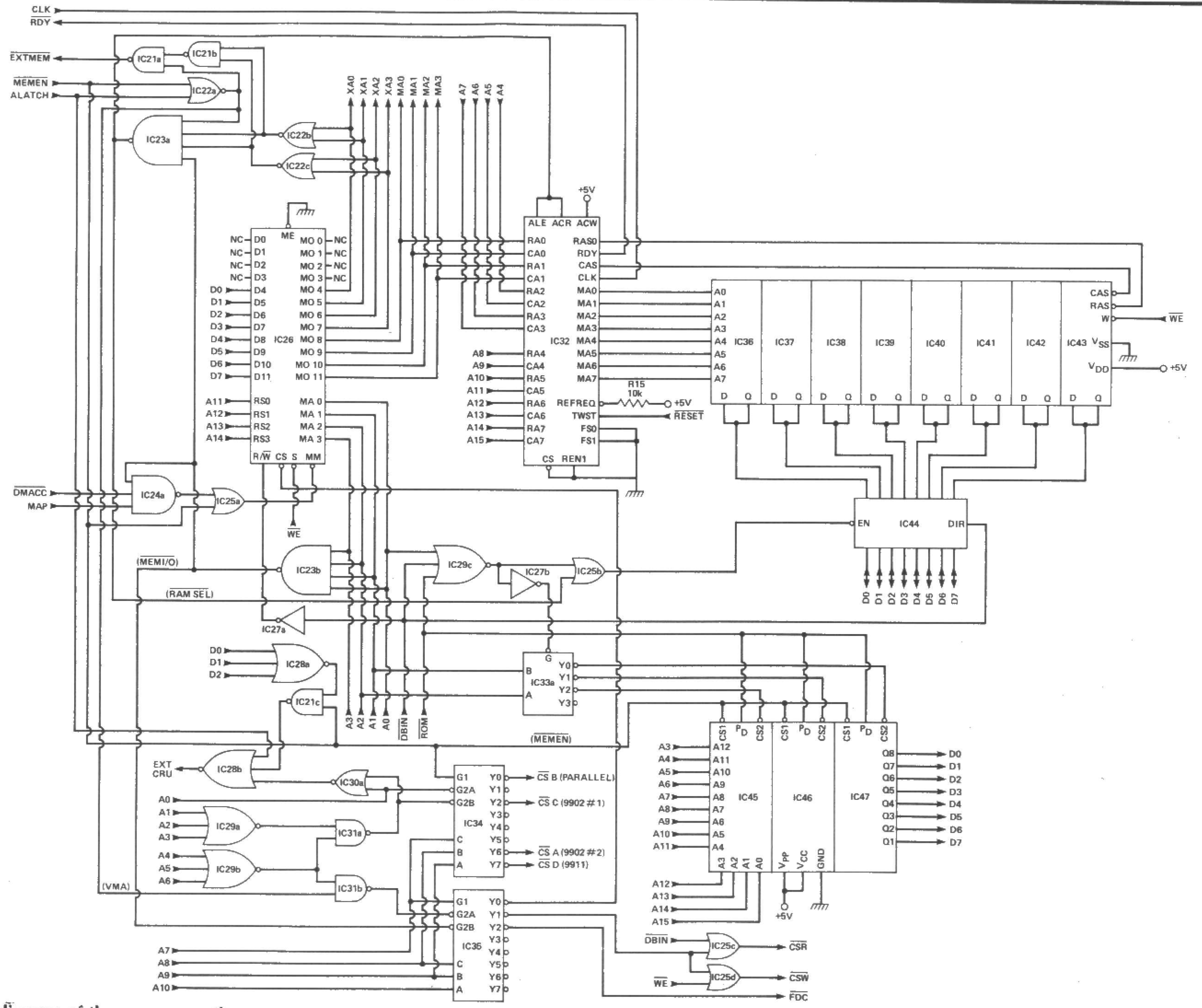


Fig. 3 Circuit diagram of the memory section.

HOW IT WORKS — MEMORY

The 24K of EPROM (IC45, 46, 47) contains the assembly language support and the BASIC interpreter. The EPROMs are switched in and out of the memory map by the I/O bit 'ROM' (see I/O section). This signal powers up in the active (low) state, with the EPROMs on. The DRAM (ICs 36–43) is also accessed during a read of the EPROMs but the data buffer IC44 is not enabled; this means that any write while the EPROMs are on is put into the DRAM, so that it behaves as a 'phantom' or ghost. The BASIC interpreter copies itself into the DRAM and then switches the EPROMs off. This has two advantages; first, during execution the interpreter overlays sections of code and then re-copies the relevant section of EPROM back to conserve memory. Second, to enable disc-based operating systems (eg Pascal) to be used, the system needs to be able to operate RAM-resident.

The addresses for DRAM accesses are passed through the memory mapper device, IC26. This segments the CPU's 64K address map into 16 pages of 4K; each page has a 12 bit register (MO0 to MO11) of which only eight bits are used (MO4 to MO11). The outputs replace the top four bits from the CPU and add four more. Thus each 4K block can be anywhere in the 1M total address reach (20 bits). The CPU at any one time still only has a 64K address map but by dynamically loading the mapper during program execution the full 1M can be used. The mapper registers are loaded or read as 16 memory locations in the memory-mapped I/O area in high memory.

The chip select logic defines the first 64K as on-board memory and the remaining memory map as off-board, using the E-BUS interface (see later). The bottom 32K of memory has the 'phantom' DRAM under the EPROM although only 24K of this is used. The DRAM occupies 60K of the memory map; the top 4K is sub-divided into 256 bytes of high-speed internal to the CPU, and then a memory-mapped I/O region for the Video Display Processor, the memory mapper and the floppy disc controller. Eight memory-mapped slots are decoded, leaving some spare chip selects for user experimentation and expansion.

The DRAM controller (IC32) takes the 16-bit least significant address signals and multiplexes them on outputs MA0–7 to supply the memory devices with the correctly-timed waveforms. Once an access request is made, the addresses are first latched and then the controller arbitrates between a refresh cycle and an access cycle. If the controller is busy refreshing the memory then it signals a 'not ready' state to the CPU on the READY line, which suspends operation until the signal returns high again. The controller has to use 'cycle-steal' refresh, as the CPU is nearly always accessing memory and not enough free time can be guaranteed. The refresh cycle obviously slows down the CPU, but by less than 10%, which is a small penalty to pay for the large amount of memory at a low cost.

a comprehensive and versatile BASIC language, high capacity devices were required. The cost and capacity trends in EPROM technology have followed a similar path to DRAMs; thus the TMS2564 was chosen to complement the TMS4164 in the system. These devices, like all the major devices in the project, operate off a single 5V rail.

Each 2564 can store 8K of program organised in the now industry-standard 8K×8 format. Three chips are used to store the firmware: 24K in all. However, an important design feature of the Cortex should be mentioned here; the EPROMs phantom the DRAMs in the memory map. At power-up the EPROMs are enabled, and after checking the DRAMs the program then copies the full operating system from EPROM into RAM. Once this has been completed the EPROMs are disabled. Thus the operating system is running in RAM, allowing changes to be made or sections deleted to create extra space. This is most noticeable when you're only operating the assembler section, since the whole of the BASIC interpreter may then be eliminated from memory, freeing an extra 20K for the user! Thus the Cortex is the only computer offering a full 64K of RAM to the user as a standard feature!

Graphic Descriptions

No home computer is considered worthy of the name these days unless it features impressive graphics capabilities, and the Cortex certainly won't disappoint you in this respect (just look at our cover and the photos in this article for some examples of the display power). What's more, all this is controlled with just one IC, the TMS9929! This chip is a memory-mapped video controller, which produces all the relevant video signals internally; it's a very versatile device capable of producing extremely complex displays, including 3D simulations. In order to achieve this its mode of operation is very different to the majority of display devices currently in use.

For simple text displays the video output of a computer may be produced by using a small random access memory to address a larger read-only memory that stores the character shape. Teletext displays fall into this category. The next step up from this is to have a display where each displayed dot is a bit (or bit pattern) stored in RAM. The first method means that shapes can be positioned very rapidly but the repertoire of shapes is limited to those in the graphics/text ROM. The second scheme is slower but allows more complex shapes to be created and lines to be plotted. However, problems occur when trying to overlay shapes as everything must be done in software — making things even slower.

The 9929 uses variants on both these schemes to produce extremely complex shapes with the minimum of software overhead. Tables are designated in an area of RAM to define pattern shapes, characters or graphics. A separate table area is designated to define attributes to the shape, such as colour and size. Finally an area of RAM akin to the Teletext RAM contains pointers for each screen location that point to the desired shape and its associated attributes. The advantage of this system is that large, dramatic changes can be made to the display very rapidly by making simple changes in the pattern look-up table. Further, all displays of one particular shape can be modified simultaneously by updating the pattern generator table.

A distinction is made in hardware between graphics and text modes, though text is available in graphics mode. They may be interchanged using the BASIC commands TEXT and GRAPH. In GRAPH mode the resolution is 256×192 (48K pixels), and the colour of each pixel can be set to any of the 16 available display colours, the only limitation being that only two colours per eight pixels may be used horizontally. To put it another way, the background may be any one of the 16 colours, while the colours of the pixels (foreground) can be set to one of 16 colours in blocks of 32×192. Control is exercised from BASIC using the COLOUR and PLOT commands.

In TEXT mode the screen format is 24 rows of 40 characters per row, each character being defined by a 6×8 bit matrix. In this case an attribute table is not required; instead the character colour is defined by a colour register on the 9929 itself that stores one foreground and one background colour. The character shapes are held in RAM in the VDP's memory

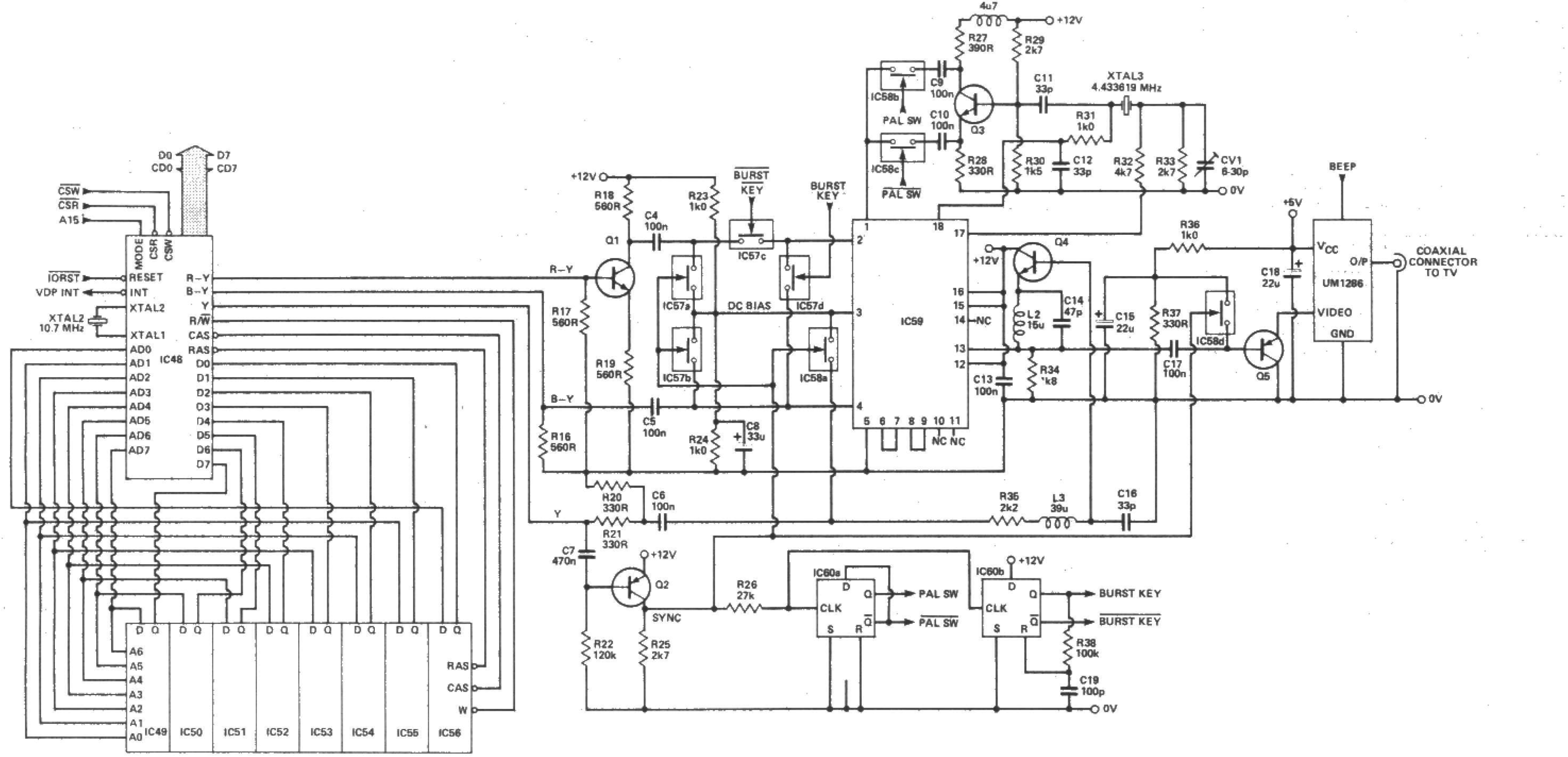


Fig. 4 Circuit diagram of the video display circuitry.

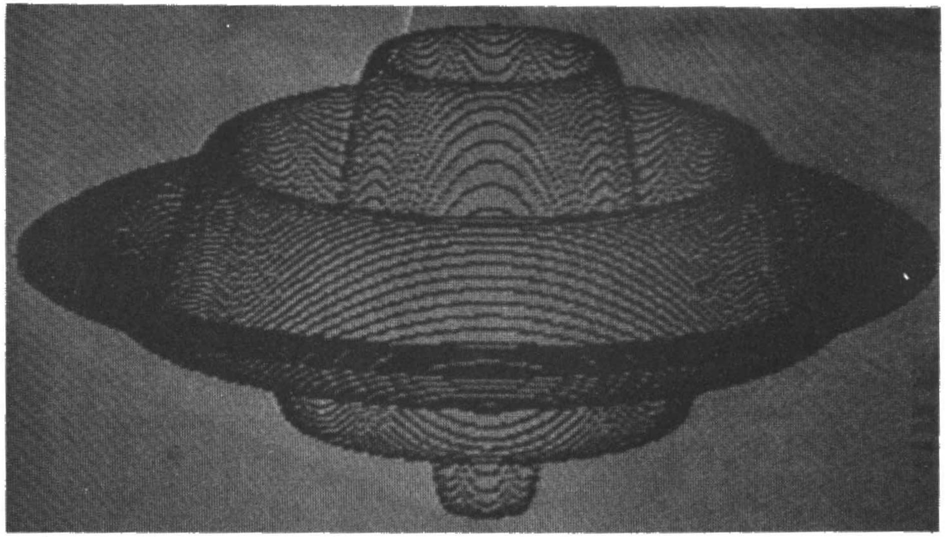
HOW IT WORKS — VIDEO DISPLAY PROCESSOR AND PAL ENCODER

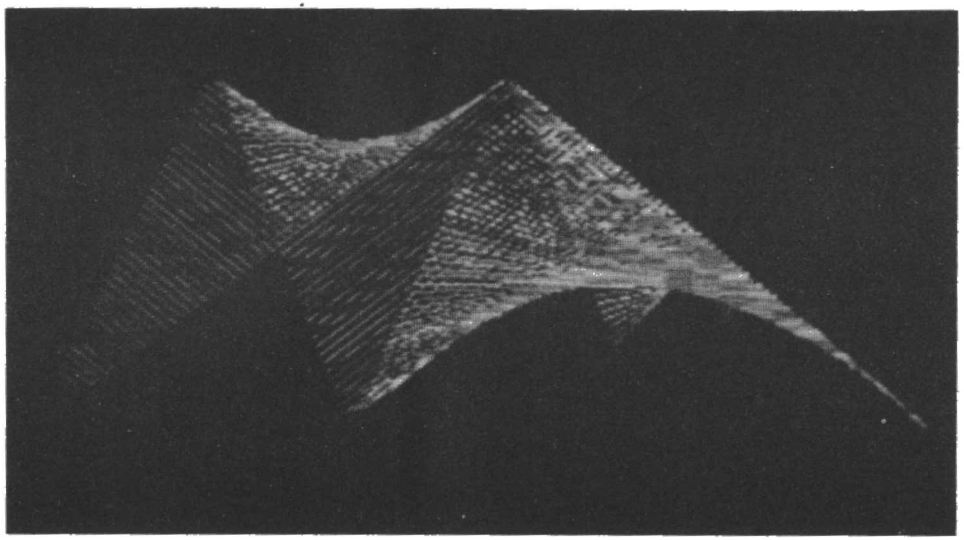
The TMS9929 (IC48) is a 625-line non-interlaced video display processor; it directly drives 16K of memory which is completely separate from the main CPU memory. The VDP fetches data from its DRAM (ICs 49-56) at such a rate that the DRAM is automatically refreshed many times over. There's very little else to say about this section of the circuitry — IC48 does everything internally! The VDP outputs a composite luminance and sync waveform on the Y output and colour difference signals on the R-Y and B-Y outputs. These signals contain all the information needed to produce either R-G-B or PAL-encoded colour. The VDP is controlled by a two-byte memory-mapped slot in high memory.

The sync is separated from the Y (luminance) signal by Q2 and associated circuitry, and used to drive DC restoration clamps IC57a,b,58a; these charge capacitors C4, 5, 6 to a reference voltage during the sync pulse. The sync is also used to toggle the PAL (Phase Alternate Line) switch, IC60a, which gates an inverted or non-inverted chroma oscillator signal into one of the two analogue multipliers in IC59. The chroma oscillator is built around Q3 and XTAL3, a crystal whose resonant frequency is 4.433619 MHz, that of the PAL colour subcarrier. The non-inverted signal is taken from the collector of Q3 via C9 and IC58b, while the inverted signal is taken from Q3 emitter via C10 and IC58c.

The second flip-flop, IC60b, is used as a monostable which, at the beginning of each line, connects the burst pulse which occurs on the B-Y signal to the R-Y input of IC59. This switching is done by IC57d. The inverting amplifier Q1 on the R-Y line from the VDP, IC48, is to match the direction of the burst pulse with the direction of the video signal to yield the correct colours.

The luminance signal is low-pass-filtered by R28, L3, C16 and then summed with the chrominance output of IC59 via the chroma trap L2, C14; this filter removes colour fringing effects. The signal is then DC-shifted by another DC restoration clamp (IC58d) to feed the RF modulator.





and so may be easily user-modified. The CHAR command allows any of the 256 possible character definitions to be altered.

Table 1 shows the 16 colours which are available; this 'palette' has been arranged to give not only a good colour display, but also a good monochrome display, as the colours produce an even grey scale on a black-and-white TV. Eight grey levels are generated.

One peculiarity may have caught your eye in Table 1: what is the point of a transparent colour? A transparent object will allow you to see what's behind it, but in most graphic displays 'behind' is meaningless. However, the VDP in the Cortex considers its display to consist of 36 planes prioritised one above the other. When you look at the screen you're seeing an image which can be considered analogous to holding 36 colour slides, one above the other in a stack, and peering through them all.

The rearmost plane is black to allow images to be built up over it. The next plane is for external video and need not concern us here. On top of this is the backdrop plane which lies directly behind the text/graphic plane. This defines the border colour as well. Since this plane defines the colour of the whole screen, it is now obvious that the only way to see the external video input or the black rearmost plane is to set the backdrop to transparent. The text/graphic plane is written to by the TEXT and GRAPH commands discussed earlier.

This leaves another 32 planes sitting in front of the four mentioned above; these are called the sprite planes. A sprite is a graphic shape that can be user-defined from BASIC with the SPRITE command. Sprites can be displayed in a variety of sizes depending on the size and magnification flags; these give four possible modes. SIZE 0 means that a block of 8×8 bits is used to define the sprite, while SIZE 1 uses 16×16 bits (but reduces the total number of different shapes from 256 to 64). The display size can be varied with the MAG command; MAG 0 maps one bit in the shape onto one pixel while MAG 1 maps one bit onto a 2×2 block of pixels on the screen.

Each sprite has four attributes associated with it; its plane (or priority), its colour and its X and Y screen coordinates. Again, each sprite can be one of 16 colours, and those bits set to 1 in the sprite definition adopt the defined colour while the other bits are set to transparent. The screen coordinates define the position of the top left-hand corner of the sprite, and sprite positions can therefore be rapidly changed by simply altering two bytes in memory. The colour can be changed equally quickly by altering one byte. Because the planes are prioritised, 0 to 31, if any shape is positioned coincident with another shape, only the one with the highest priority plane will be displayed. This gives rise to simple 3D simulation. A status flag is set to indicate when any two sprites 'touch' each other. Any point in the text or graphic plane will only be seen if all the points directly above it on the 32 sprite planes are transparent.

All these features mean you can generate very versatile and complex displays; but they also use up a reasonable amount of memory. We don't believe that screen RAM should be stolen from the user RAM, so the VDP only occupies two bytes in the CPU memory map. These two registers are all that's required to write all the relevant information through the VDP chip and into its own 16K of DRAM.

More next month!

TABLE 1

Code	Colour	Code	Colour
0	transparent	8	medium red
1	black	9	light red
2	medium green	10	dark yellow
3	light green	11	light yellow
4	dark blue	12	dark green
5	light blue	13	magenta
6	dark red	14	grey
7	cyan	15	white

BUYLINES

Powertran are supplying complete kits of parts and component packs for the Cortex. A complete 64K Cortex kit will cost £295 plus VAT, carriage free. A ready-built 64K Cortex will cost £395 plus VAT, carriage free. Prices for add-ons (eg floppy discs, RS232C interface, memory expansion etc) and for component packs (eg PCB, semiconductors etc) can be found in Powertran's brochure. Powertran Cybernetics, Portway Industrial Estate, Andover, Hants SP10 2NM. Telephone 0264 64455.

CONFIGURATIONS

Most readers will be familiar with the three types of multivibrator in the form of ICs (for example, the 555 and 4013). Here Ian Sinclair shows how it's done with just a couple of transistors.

The multivibrator is a circuit of remarkable antiquity — it is attributed to Abrahams and Bloch at around 1918. Over the years, as various valve and subsequently transistor versions were devised, a variety of names were attached to them. However, the names astable, monostable and bistable are particularly useful as descriptions of the various multivibrator circuits.

The astable is a circuit which oscillates continually (no stable state — hence the name), producing steep-sided waveforms whose frequency can be adjusted by changing RC time constants. The monostable has only one stable state, and an input pulse will disturb this state for a time that depends on the time constant of the circuit, following which it returns to the stable waiting state. This circuit is widely used as a pulse generator, because ideally the duration of the pulse (the pulse-width) is independent of the repetition rate of the pulse, which is determined by the rate at which the monostable is triggered. The bistable circuit (two stable states) is the basis of digital circuitry, but is seldom used in discrete form nowadays because of the low cost of digital ICs. A source of confusion over names, incidentally, has been the use of 'flip-flop' by digital circuit designers, whereas the name was traditionally used to mean a monostable.

Astable Antics

Two varieties of astable exist, the parallel and the serial, of which the parallel is much the better known. The basic circuit is shown in Fig. 1, but unless your needs are very simple, the waveform from this circuit is not really good enough without reshaping. A much better circuit is shown in Fig. 2; this uses a diode to isolate the collector from which the output is taken. When Q2 cuts off, its collector voltage can rise sharply, leaving D1 reverse biased. In the simple circuit, a sharp rise of voltage at the collector of Q2 is made impossible by the capacitor C2 which has to be charged through the collector load resistor (R4 in Fig. 1). By using the diode, the collector voltage can rise sharply, and the charging of C2 is done at a slower rate by the additional resistor R5. This ensures a much sharper shape of waveform at the output.

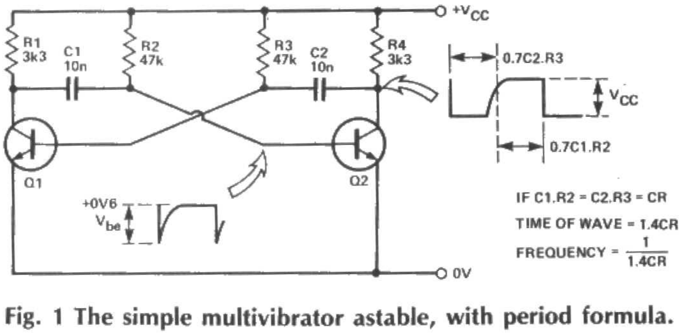


Fig. 1 The simple multivibrator astable, with period formula.

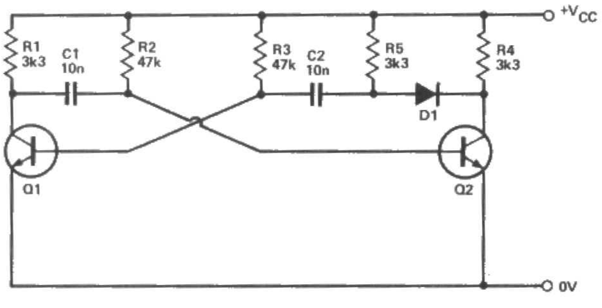


Fig. 2 Using an isolating diode to sharpen the leading edge.

Another problem of the simple circuit is that, contrary to theory, its frequency changes as the supply is changed. This is because silicon planar transistors will conduct readily in the reverse direction when the base voltage is negative with respect to the emitter (for an NPN transistor). This is a form of zener breakdown, but it can be prevented by connecting silicon diodes with a higher reverse breakdown voltage in series with the base leads, as shown in Fig. 3, so greatly improving the frequency stability of the astable.

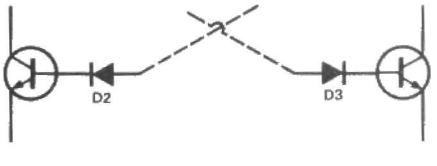


Fig. 3 Using base-isolating diodes to prevent base-emitter breakdown.

Formula For Success

The astable frequency is given by the formula shown in Fig. 1 — it depends on the two sets of time constants. These should not be greatly different — don't be tempted to try to produce pulses with very large or very small values of mark-to-space ratio by using an astable with very different values of the two time constants. The waveform will probably be disappointing, and the circuit may not start oscillating reliably.

The frequency stability of an astable is generally poor compared with that of the LC type of oscillator, and this feature makes the astable particularly useful inasmuch as it can be easily synchronised to external pulses. Unless the 'natural' frequency of the astable is reasonably close to the incoming frequency, however, synchronisation cannot be relied on, and slowly-changing waves such as sinewaves are not useful for synchronisation because the triggering point is liable to vary (or jitter) from one wave to the next. The astable can be synchronised by pulses at one base, and this can be done by pulsing a cut-off base into conduction or by pulsing a conducting base to cut-off.

Whichever method is used, the trigger pulse should be isolated from the astable by diodes to prevent the astable interfering with the action of the trigger circuit (Fig. 4). If the 'pulse-off' method is used, a catching diode must be included to prevent the transistor base-emitter junction from being reverse-biased which would cause zener action on each negative pulse.

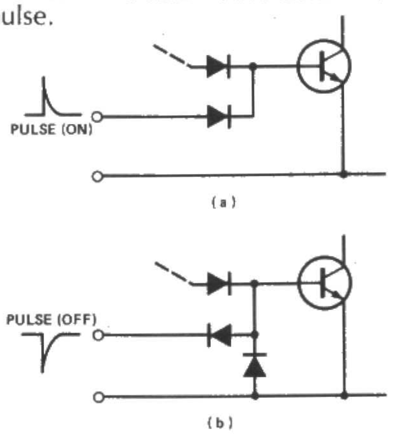


Fig. 4 Diodes are used in the synchronising circuits, too!

Breakfast Serial?

The other type of astable, much less well known, is the serial astable, which is a particularly good way of producing very short pulses which can pack a lot of energy. A circuit is shown in Fig. 5, and since the circuit is not so familiar as that of the parallel astable, a run through its action might be of interest. Note that only one time constant, R1.C1, is used, and that the transistors are complementary; one PNP, one NPN.

We can start by supposing R2 = R3 and V_{cc} = 10 V, with C1 discharged so that the emitter of Q1 is at a low voltage. Q1 will be cut off, and will stay that way until its base voltage is more negative than its emitter voltage, or to put it another way, until its emitter voltage rises to more than its base voltage. With the base voltage fixed at +5 V by R2 and R3, the capacitor will have to charge to around 5V6 before much will happen.

Meantime, because Q1 cut off, no current is reaching the base of Q2, and this transistor also is cut off. The circuit remains with neither transistor conducting until the charging capacitor reaches the voltage at which Q1 turns on. This also turns on Q2, because the collector current of Q1 goes to the base of Q2. This in turn drastically lowers the base voltage of Q1, and the emitter voltage will follow it, rapidly discharging C1. Once the emitter voltage of Q1 drops, however, the circuit recovers, and we're back where we started.

Unlike the parallel circuit, in which one transistor conducts while the other is cut off, the serial multivibrator spends most of its life with both transistors cut off, and only brief intervals with both turned on. The cut-off time is the time needed to charge C1 through R1 to about 0V6 above the voltage supplied by R2 and R3 — the formula for the time is shown in Fig. 5. The time for which both transistors are on is less easy to estimate because it depends on the effective resistance of the transistors at saturation; it is normally very short compared to the charging time.

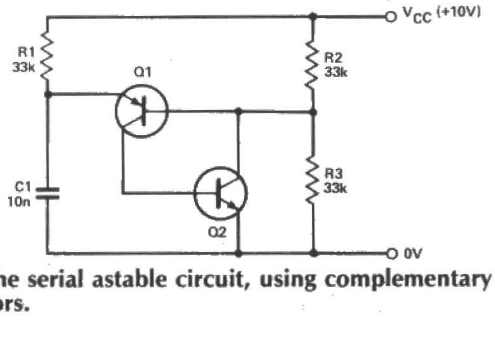


Fig. 5 The serial astable circuit, using complementary transistors.

Monostables

The classic monostable uses a parallel circuit with one DC coupling, as shown in Fig. 6. With no trigger-pulse input, Q2 is held on because of current flowing through R2. The collector voltage of Q2 is very low, and this ensures that Q1 is held off. This is the stable state of the circuit, and it wil remain in this condition, with C1 charged, until a positive-going trigger pulse arrives, with enough amplitude to make Q1 conduct. This pulse causes current to flow in Q1, so that the collector voltage drops, and the drop in voltage at the base of Q2 cuts Q2 off. This condition lasts until C1 charges through R2 sufficiently to turn the base of Q2 on again, when the circuit switches back. The diode in the base lead of Q2 prevents base-emitter breakdown from affecting the timing.

As in all parallel circuits, there is always one transistor conducting and the other cut off. The serial version of the monostable (Fig. 7) uses complementary transistors, and will pass no current in its waiting state. When a trigger pulse arrives, Q2 switches on, and the voltage at its collector drops. This switches on Q1, via the capacitor C1, causing the base circuit of Q2 to be heavily forward biased. C1 now charges through R2 until the voltage at the base of Q1 rises to its cut-off value of around V_e—0V6. Both transistors then cut off.

The pulse width of the output depends on the time constant of C1.R2, and will vary as the supply voltage varies. Diodes can be used to prevent base-emitter breakdown in the usual way.

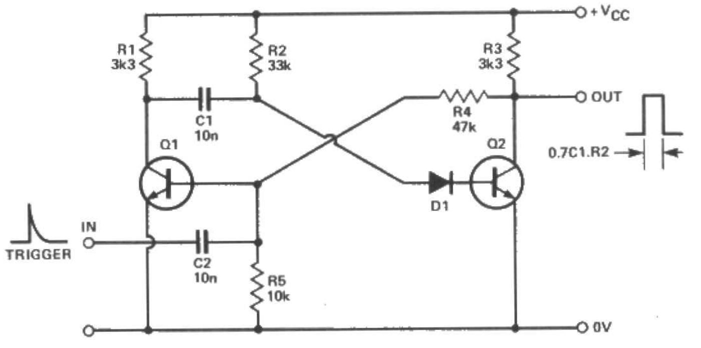


Fig. 6 The parallel monostable circuit.

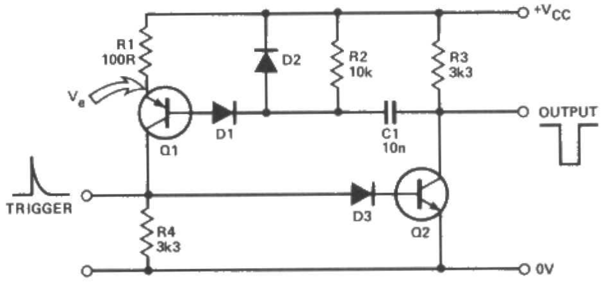


Fig. 7 A serial astable — a useful circuit which is seldom seen.

Bistables, Two By Two

Figure 8 shows the classic bistable circuit using two NPN transistors. The circuit is stable with either Q1 on and Q2 off, or in the alternate condition of Q1 off and Q2 on. Switching is done by using the A or B inputs. With Q1 on, a negative pulse at A will switch the circuit over, and a negative pulse at B will switch it back. This action corresponds to that of the simple set-reset latch.

Counting action may be obtained if steering diodes are added to the basic circuit, as illustrated in Fig. 9. Suppose Q1 is conducting: its base voltage will be around

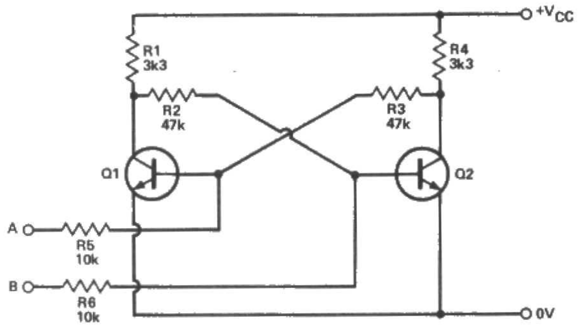


Fig. 8 The simple R-S type of bistable.

0V6, and its collector voltage about 0V1, so that D1 is almost conducting. D2 is cut off because its anode voltage will be about zero and its cathode voltage almost at supply voltage. C1 will carry virtually zero charge, while C2 will be charged to around supply voltage, V_{cc}. When a negative trigger pulse of amplitude around 1 V is applied D1 conducts, allowing Q1 to be cut off by the trigger pulse; however, D2 is held off by the charge on C2. The bistable then changes over so that Q2 is fully conducting and Q1 cut off. In this condition, it is D2 which is biased almost on and D1 completely off. When the next trigger pulse arrives, then, Q2 will be cut off by it, and the circuit will switch back to its original state. Hence, if the circuit is triggered regularly, either output will be a square wave with half the frequency of the trigger pulses.

The waveforms at the collectors of a bistable can be much closer to square than those from simple astables, so that one way of creating well shaped square waves is to drive a bistable from an astable (Fig. 10). In this circuit, the output from the bistable has the same frequency as the astable. Nowadays, the ready availability of bistables in integrated form discourages us from using the discrete variety — we'll look at IC types later in this series. **ETI**

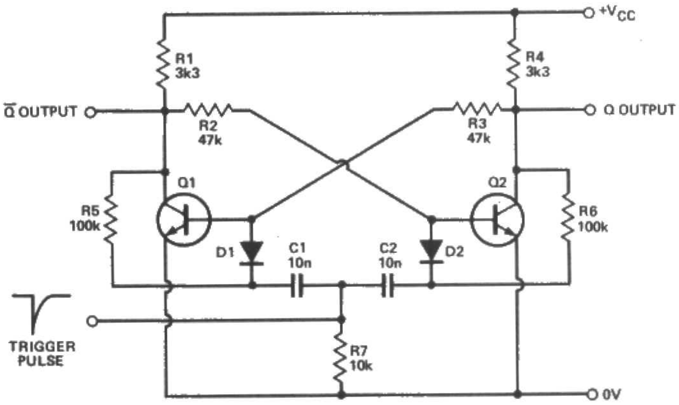


Fig. 9 A bistable with steering diodes to give the scale-of-two action.

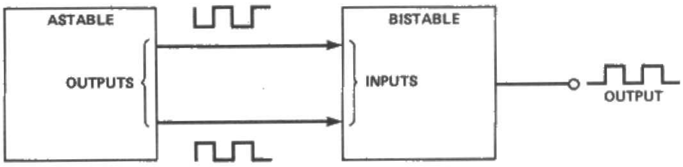


Fig. 10 Following an astable with a bistable to sharpen the waveform.

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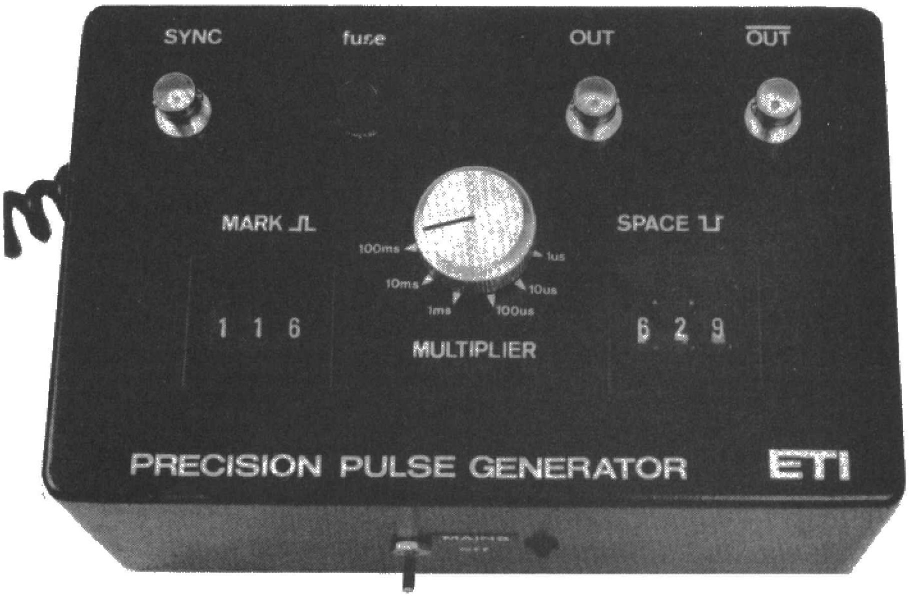
PRECISION PULSE GENERATOR

Fed up with boring, ordinary 1:1 mark/space ratio square waves? Here's a digital pulse generator that lets you stretch 'em or shrink 'em with finger-tip control. Design by Andy Elam.

The pulse generator described here is a piece of laboratory test equipment that can be built for a price that is modest when compared with equivalent commercial gear. It is a very accurate unit and has many applications.

Mark/space ratios from 1:999 to 999:1 and a wide range of frequencies can be set from the front panel. The unit delivers a clean TTL-compatible DC coupled signal, accurate to a very small fraction of a percent.

For convenience, thumb-wheel switches are used; these should be of the decade type. However, these are quite expensive, and you may possibly find these switches on sale in a surplus store.



Construction

The PCB should be assembled first. We recommend using IC sockets throughout to avoid damaging the ICs when connecting up the wires for the thumb-wheel switches, etc. Using Vero pins for the off-board connections will make life easier anyway. The voltage regulator needs a heatsink bolted on to it or it could be mounted directly on to a metal case (note that the metal tab is connected to the 0V line). Leave mounting the ICs and crystal until after the wiring is complete.

What sort of box you use to house the unit is up to you; it must, of course, be large enough for the board and all the other components. We used a die-cast aluminium box, and metal boxes such as this must **always** be grounded to the mains earth. The most troublesome part of preparing the box will probably be the cutting of the holes to take the thumb-wheel switches. However, this must be done very carefully, because otherwise the switches won't stay put. Probably the best method is to use drilling and sawing to get an under-size

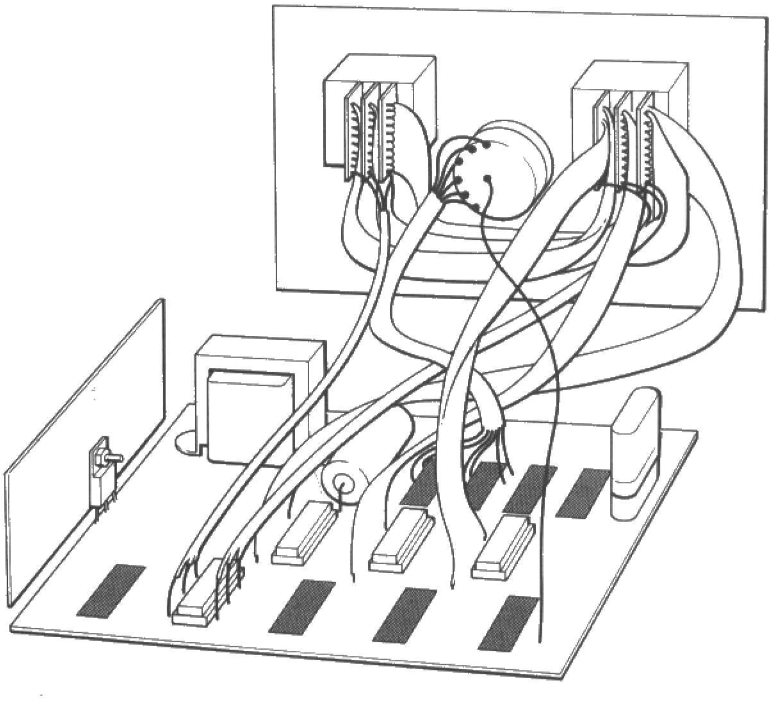


Fig. 1 Wiring diagram of board to thumb-wheel and range switches.

PARTS LIST

Resistors (all ¼ W 5%)	
R1	1k0
R2,3	470R
R4	220R
Capacitors	
C1	10n ceramic
C2,3	22n ceramic
C4	1000u 25V axal electrolytic
C5,6	100n ceramic
Semiconductors	
IC1,2,3	74LS160
IC4	74LS27
IC5	74LS00
IC6	74LS73A
IC7,8,9	74LS42
IC10	7805 5V regulator
IC11	74LS04
IC12,13,14	74LS390
BR1	bridge rectifier, 20V min
LED1	3 mm light emitting diode, colour to choice
Miscellaneous	
XTAL1	10 MHz crystal
SW1	double pole mains switch
SW2	six way switch, at least one pole
SW3-8	decade thumb-wheel switches (see Buylines)

9 V (4.5 + 4.5) 6VA transformer, end cheeks for thumb-wheel switches (4 off), fuse holder, mains plug and socket, output sockets, box, heatsink, IC sockets (16 pin, 9 off; 14 pin, 4 off) socket for crystal (optional), knobs, spacers for PCB, PCB.

BUYLINES

The thumb-wheel switches may be source of trouble, though there are several possible suppliers. As these switches are quite expensive, it will be worth trying your local friendly surplus store for them.

HOW IT WORKS

The circuit is a variable frequency clock linked to a counter with variable end-stops. The master oscillator is based on a 10 MHz crystal, XTAL1. Crystal control was chosen because of the vastly superior accuracy and stability it offers over other methods. The output from the oscillator is sent down a chain of decade dividers, ICs 12a, b, 13a, b, 14a, b. SW2 selects which frequency is passed on to the counter section.

The counting section divides the output selected by SW2 by 10 three times over, so that the carry-out output from IC1, were it used, would be 1/1000th frequency of the input selected from SW2. The BCD outputs from IC1, 2, 3 are converted to decimal by IC7, 8, 9 (note that the numbers next to the right hand sides of these ICs are the pin numbers) and these are fed to the thumb-wheel switches, SW3-8. IC4a and b sense when the outputs of all their thumb-wheel switches go low and one of their outputs will instantaneously go high when this happens. The pulse from either IC5a or b is fed through IC5c and d, and used to do two things: to reset all the decade counters, and to toggle the flip-flop, IC6. Thus if IC5a was responsible for the reset pulse, the next reset pulse must come from IC5b. So, when OUT is high SW3, 4, 5 are effectively disabled and the counters will count until they reach the setting on SW6, 7, 8; similarly when $\overline{OUT}$ is high SW6, 7, 8 are disabled and the counters will count until they reach the setting of SW3, 4, 5. Thus alternate counts are to the settings on the two banks of thumb-wheel switches. The SYNC output can be used to synchronise an oscilloscope to the output pulses.

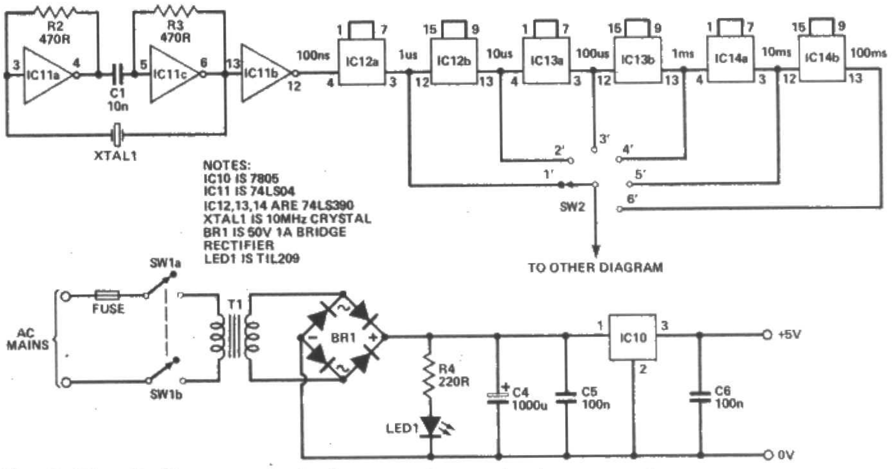


Fig. 2 Circuit diagram of clock generator and power supply.

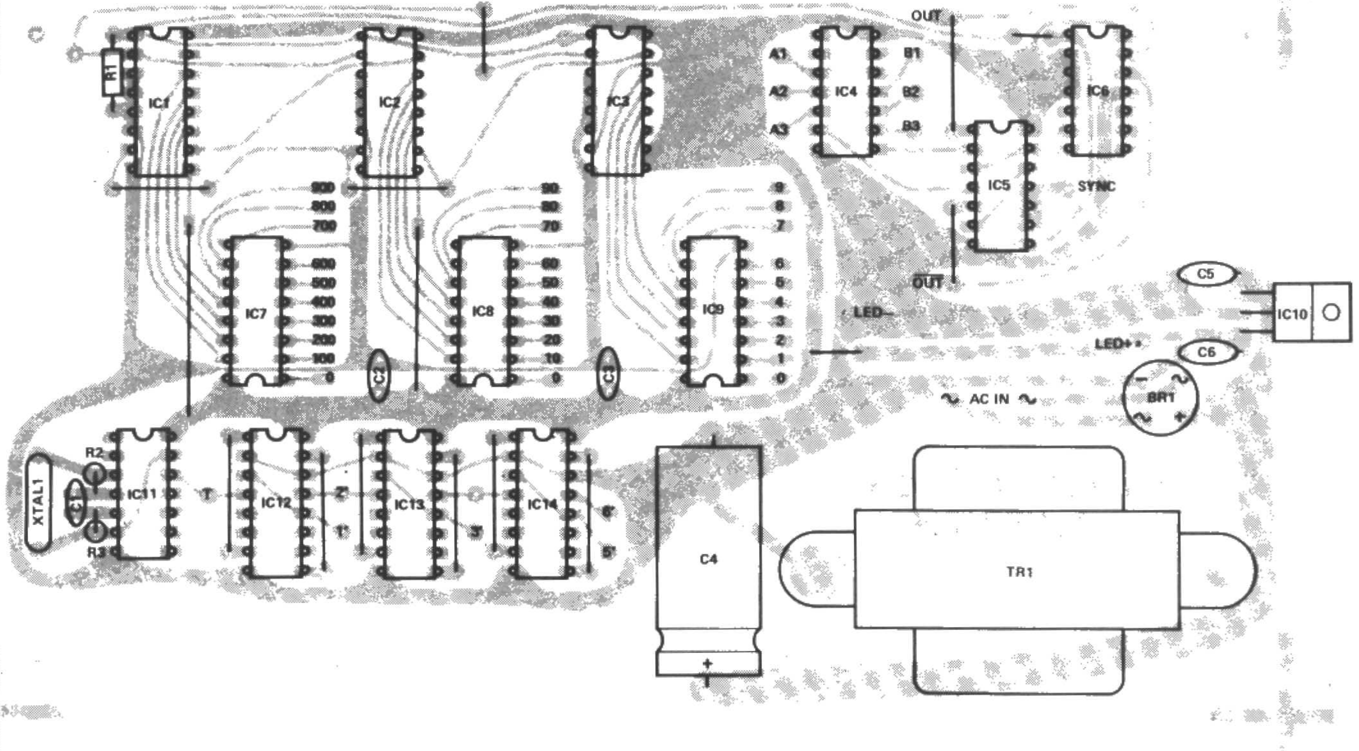
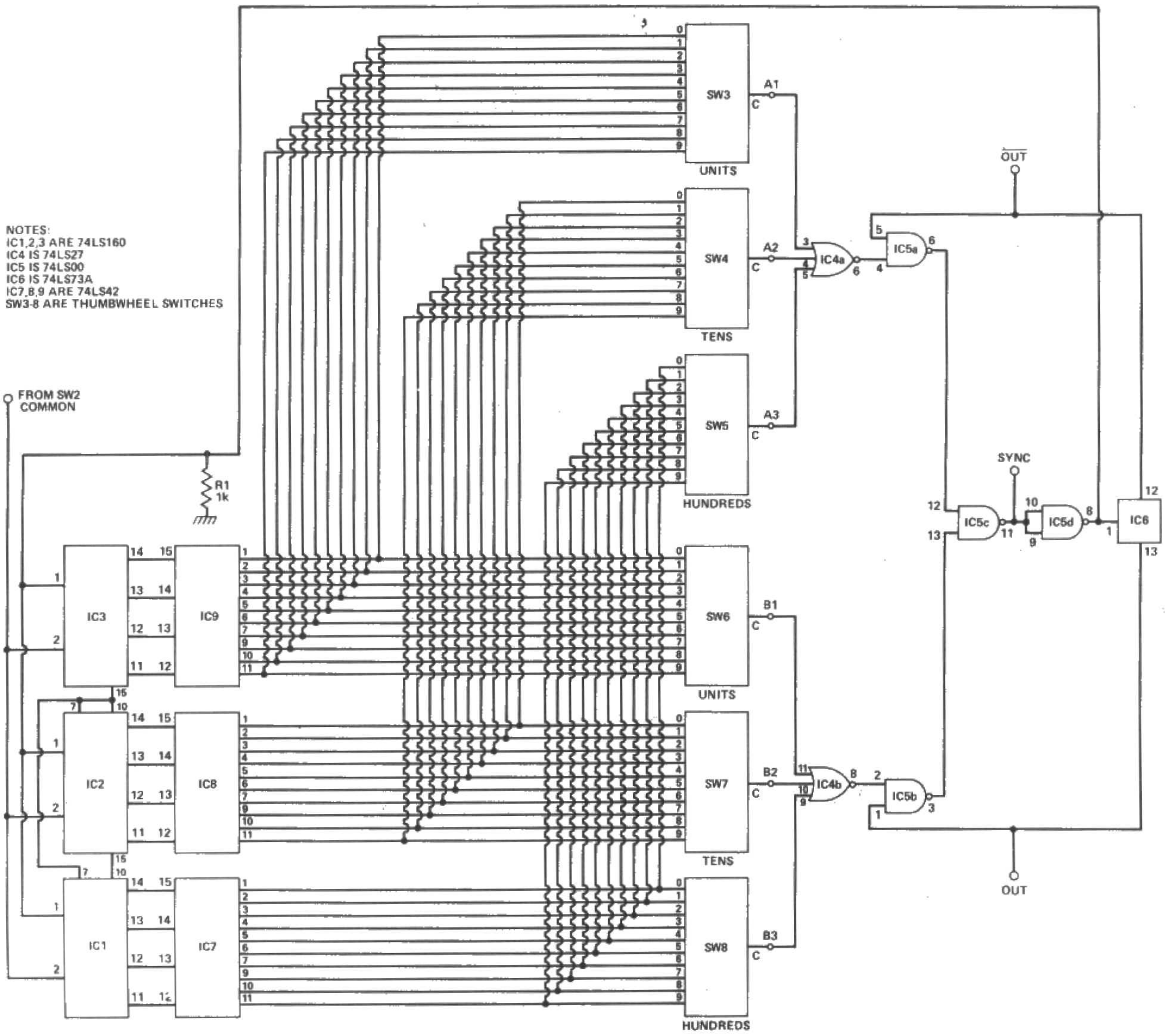


Fig. 3 Overlay diagram.



NOTES:
IC1,2,3 ARE 74LS160
IC4 IS 74LS27
IC5 IS 74LS00
IC6 IS 74LS73A
IC7,8,9 ARE 74LS42
SW3-8 ARE THUMBWHEEL SWITCHES

Fig. 4 Circuit diagram of counter section.

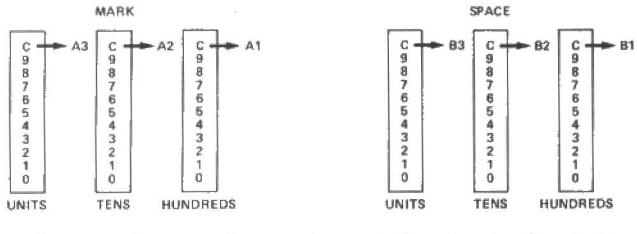
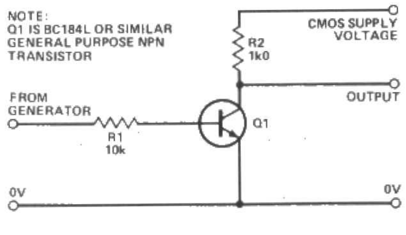


Fig. 5 Details of connections and mounting of thumb-wheel switches.

SPECIFICATIONS

Minimum pulse width:	1 uS
Maximum pulse width:	99.9 S
Six multiplying ranges:	×1 uS ×10 uS ×100 uS ×1 mS ×10 mS ×100 mS
Minimum mark/space ratio:	1:999
Maximum mark/space ratio:	999:1
Output level:	Mark, 4 V Space, 0 V

Rise time: better than 10 nS
Fall time: better than 10 nS
Fan-out: up to 16 low power Schottky loads



NOTE:
Q1 IS BC184L OR SIMILAR GENERAL PURPOSE NPN TRANSISTOR

Fig. 6 A simple level shifter circuit that can be used to drive CMOS or similar operating at 12 V or 15 V; note that this circuit inverts the signal, so use $\overline{\text{OUT}}$ rather than OUT or vice-versa.

hole, then carefully finish off using a flat file.

Wiring up the thumb-wheel switches should present few problems if colour-coded ribbon cable is used. The resistor colour code can be handy for sorting out what all the wires are — eg, use black for 0, brown for 1, etc.

Connect the crystal and insert the ICs, and, after a careful check to ensure that all the components and connections (particularly the mains connections, the electrolytic capacitor and ICs) are where they should be and the right way around, you should be ready to switch on and go! If any problems develop, the first point to check is that the master oscillator is running, and after that the divide-by-10 counters in the clock generator are running (though this does assume that you have checked the fuse).

ETI

DESIGNER'S NOTEBOOK

Switched capacitor filters might appear to be unsuitable devices for anyone who isn't an expert. Tim Orr looks at them and finds that they are really much easier to use than conventional filters.

Most complex filter designs require a large number of precision resistors, inductors and capacitors. Resistors and capacitors are relatively easy to integrate, and inductors can be synthesised using an op-amp plus capacitors and resistors. Thus it would seem possible to produce a monolithic active filter, but there is one major problem. The accuracy of monolithic capacitor values is typically fairly low, and constructing multi-pole filters requires good matching between stages: a sixth order low-pass filter would typically require a component tolerance of 1 or 2%. Additionally, monolithic capacitors and resistors are limited to fairly low values, though this could be designed around.

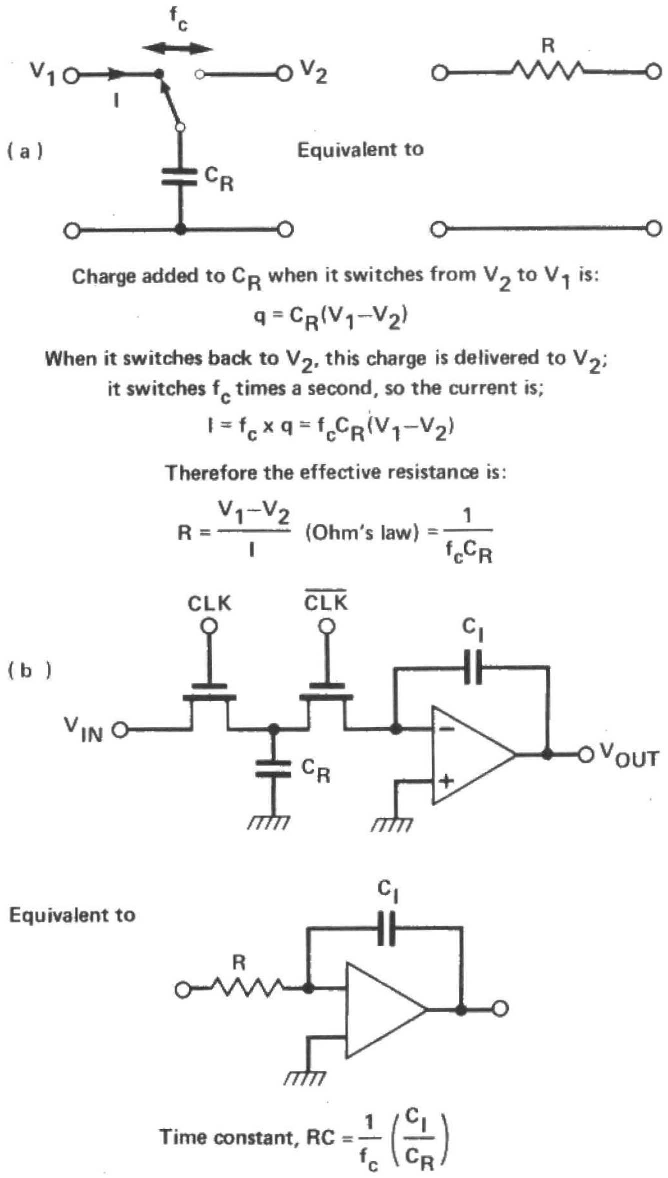
Switched capacitor techniques get over these problems by using a capacitance to synthesise a resistance; see Fig. 1. The resistance is synthesised by switching charge into and out of the capacitor C_R, as the MOSFET switches open and close in antiphase; the average current passing from the input to the op-amp (and hence the apparent resistance) depends on the switching frequency. This helps because the *ratio* of the values of two monolithic capacitors on the same IC can be accurately controlled (to 1% or better). In the simple example of a low-pass filter shown in Fig. 1, the break frequency is proportional to the switching frequency and the ratio of the capacitor values. Switched capacitor filters are normally designed this way (even the very complicated ones). The switching frequency is usually arranged to be around either 50 or 100 times the break frequency of the filter, and therefore only very simple anti-aliasing and recovery filtering are required.

Several manufacturers produce switched capacitor filter ICs and all the classic filter structures are available. These devices offer several advantages over conventional passive and active filters:

- filters can be made very compact
- very few external components are needed
- the filters are tunable by adjusting the externally generated sampling frequency — so no re-alignment is necessary when break-frequencies are changed
- circuit calculations are made very easy.

The following section is a review of some of the currently available devices. Next month, we'll look at a few examples of practical filter circuits using switched capacitor ICs.

ETI would like to thank the manufacturers mentioned in this article for their permission to reproduce the information given on their data sheets.



Charge added to C_R when it switches from V_2 to V_1 is:

$$q = C_R(V_1 - V_2)$$

When it switches back to V_2, this charge is delivered to V_2; it switches f_c times a second, so the current is;

$$I = f_c \times q = f_c C_R (V_1 - V_2)$$

Therefore the effective resistance is:

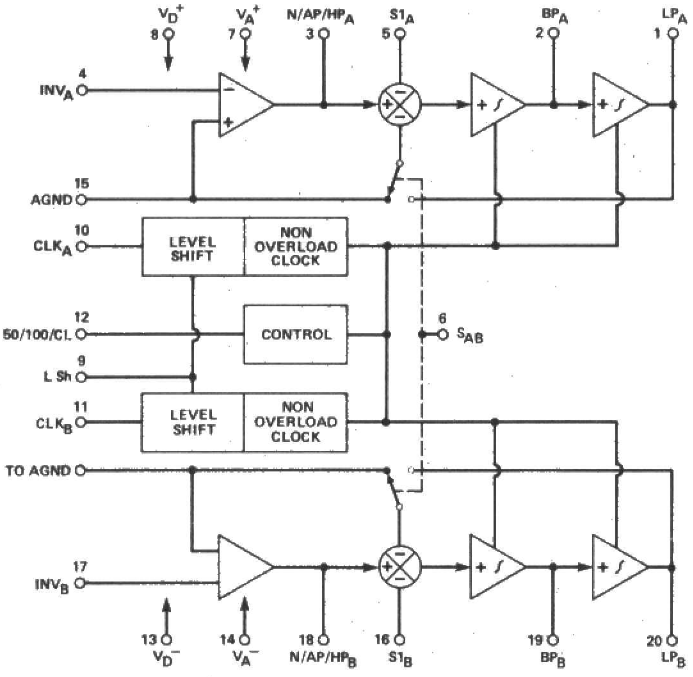
$$R = \frac{V_1 - V_2}{I} \text{ (Ohm's law)} = \frac{1}{f_c C_R}$$

Time constant, $RC = \frac{1}{f_c}\left(\frac{C_I}{C_R}\right)$

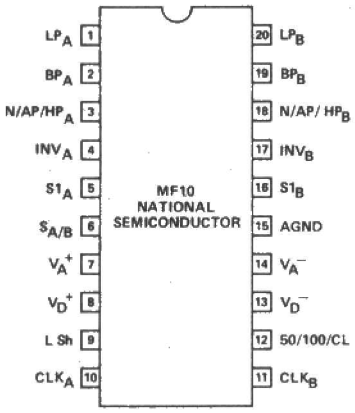
Fig. 1 Basics of switched capacitor filters. Synthesising a resistance (a); a simple low-pass filter using a synthesised resistance (b).

MF10 — National Semiconductor

The MF10 is a dual independent active filter building block. Virtually any classic filter structure can be fabricated with this device.



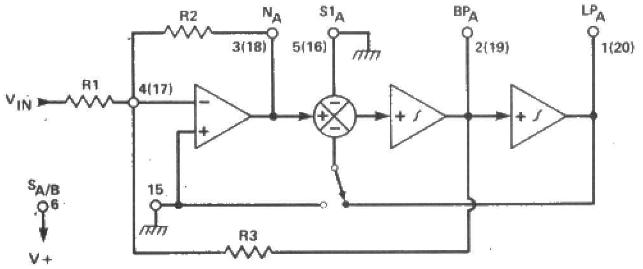
DUAL-IN-LINE PACKAGE



TOP VIEW

SUPPLY VOLTAGE ± 5V

LP, BP, N/AP/HP	low-pass, band-pass, notch, all-pass and high-pass outputs respectively. All can sink 1 mA and source 3 mA; N/AP/HP can sink 1.5 mA	L Sh	level shift for clock inputs. For TTL input, tie to 0 V; for CMOS operated from 10 V, tie to negative supply rail
		CLK A or B	clock inputs for each filter unit
V_A+, V_D+	positive analogue and digital supply rails. These are linked internally, and so must have the same supply voltage applied to them, normally +5 V	50/100/CL	defines relationship between clock frequency and filter centre frequency; tie to positive supply for 50:1 ratio, tie to 0 V for 100:1
V_A−, V_D−	negative supply rails, also internally connected; normally −5 V	$S_{A/B}$	activates internal switches, see section on use; note that there is only one $S_{A/B}$ for both filters
AGND	analogue ground, which should be at 0 V, ie mid way between positive and negative supply rails		



MODE 1

MODE 1: Notch 1, Band-pass, Low-pass outputs: $f_{notch} = f_o$

f_o = centre frequency of the complex pole pair

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_{notch} = centre frequency of the imaginary zero pair = f_o

H_{OLP} = Low-pass gain (as $f \to 0$) = $\frac{R2}{R1}$

H_{OBP} = Band-pass gain (at $f = f_o$) = $-\frac{R3}{R1}$

$$H_{ON} = \text{Notch output gain as} \left\{ \begin{matrix} f \to 0 \\ f \to f_{CLK}/2 \end{matrix} \right\} - \frac{R2}{R1}$$

$$Q = \frac{f_o}{BW} = \frac{R3}{R2}$$

= quality factor of the complex pole pair.

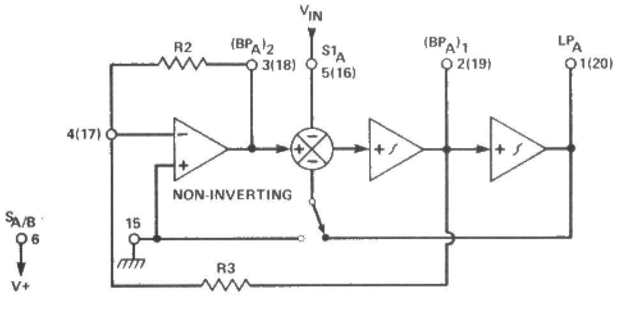
BW = the −3dB bandwidth of the band-pass output.

Circuit dynamics:

$$H_{OLP} = \frac{H_{OBP}}{Q} \text{ or } H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q.$$

$$H_{OLP(peak)} = Q \times H_{OLP} \text{(for high Q's)}$$

The above expressions are important. They determine the swing at each output funtion of the desired Q of the 2nd order funtion.



MODE 1a

MODE 1a: Non-inverting BP, LP.

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

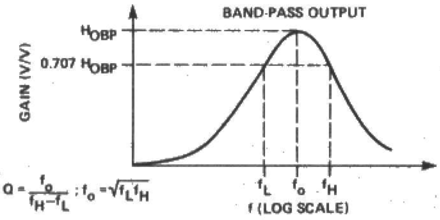
$H_{OLP} = 1$; $H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$$H_{OBP_1} = -\frac{R3}{R2}$$

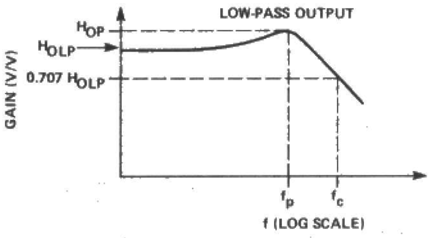
$H_{OBP_2} = 1$ (non-inverting)

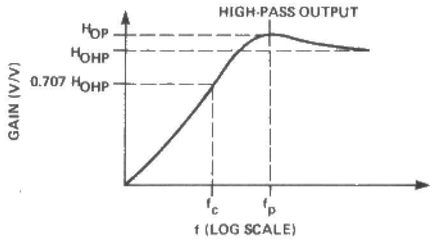
Circuit dynamics: $H_{OBP_1} = Q$

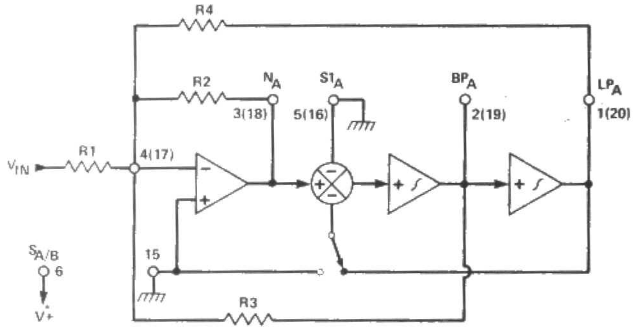
Definition of terms



$Q = \frac{f_o}{f_H - f_L}$; $f_o = \sqrt{f_L f_H}$







MODE 2

MODE 2: Notch 2, Band-pass, Low-pass: $f_{notch} < f_o$

f_o = centre frequency

$$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

Q ≈ quality factor of the complex pole pair

$$= \frac{\sqrt{R2/R4+1}}{R2/R3}$$

H_{OLP} = Low-pass output gain (as $f \rightarrow 0$)

$$= -\frac{R2/R1}{R2/R4+1}$$

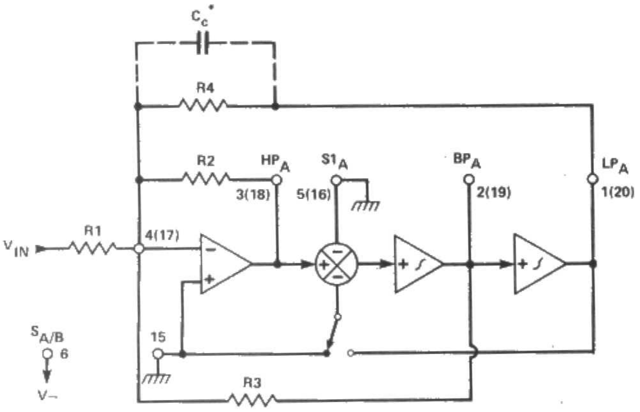
H_{OBP} = Band-pass output gain (at $f = f_o$) = $-R3/R1$

H_{ON_1} = Notch ouput gain (as $f \rightarrow 0$)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{ON_2} = Notch output gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}H_{ON_2}} = Q\sqrt{H_{ON_1}H_{ON_2}}$



MODE 3

* In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10pF-100pF) across R4 to provide some lead.

MODE 3: High-pass, Band-pass, Low-pass outputs

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R2}{R4} \times \frac{R3}{R2}}$$

H_{OHP} = High-pass gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$

H_{OBP} = Band-pass gain (at $f = f_o$) = $-\frac{R3}{R1}$

H_{OLP} = Low-pass gain (as $f \rightarrow 0$) = $-\frac{R4}{R1}$

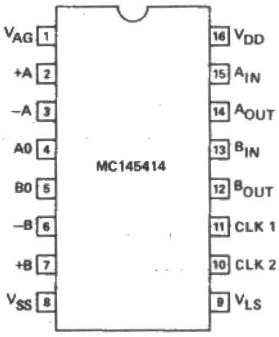
Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$

$H_{OLP(peak)} = Q \times H_{OLP}$ (for high Q's)

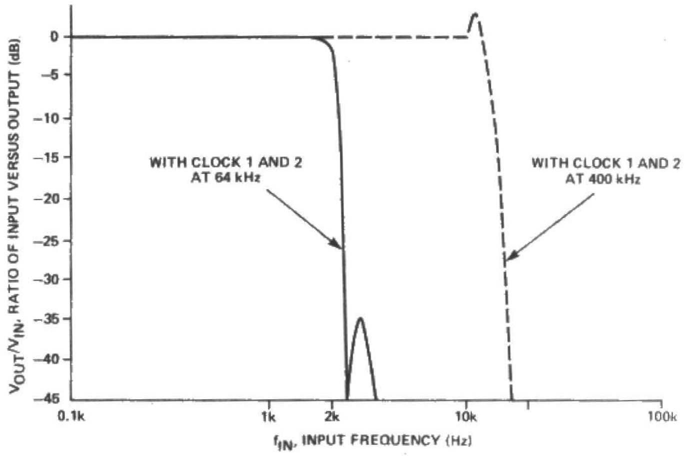
$H_{OHP(peak)} = Q \times H_{OHP}$ (for high Q's)

MC145414 — Motorola

This is a dual low-pass filter which can operate with a break frequency between 1.25 and 10 kHz. It also contains two completely uncommitted op-amps in the same package. Filters are fifth-order elliptic, and have a clock-to-break-frequency ratio of approximately 36:1 (clock frequency must be between 50 and 400 kHz). Filter A has 18 dB gain in the pass band, while filter B has unity gain. The clock input voltage may be selected to be 5 V or 12 V, or the whole IC may be powered down by the application of suitable supply voltages.



V_{AG}	analogue ground; all analogue signals are referred to this level, and it should normally be around mid-way between positive and negative supply rails. If taken to within 1 V of positive rail, IC will power down	V_{LS}	logic shift voltage; for TTL clock input, take to mid-way between supply rails; for CMOS operating on to 12 V, take to negative supply rail. To power down IC, take to positive supply rail
+A, −A, AO	non-inverting, inverting inputs, and output of op-amp A	CLOCK 1, 2	clock inputs — should always be tied together
+B, −B, BO	as above for op-amp B	A_{IN}, B_{IN}	inputs to filters A, B
V_{DD}, V_{SS}	positive and negative supply rails. V_{SS} is also ground for digital inputs	A_{OUT}, B_{OUT}	outputs from filters A, B



R5620 — Reticon (not illustrated)

This device is a switched capacitor universal active filter, with digital setting of both the Q-factor and the filter centre frequency. It is a second order filter capable of high-pass, low-pass, band-pass, notch and all-pass. The filter frequency is determined by the clock frequency and a five-bit binary input that moves the frequency over a two-octave spread in 32 logarithmically spaced intervals. This enables direct digital control of the centre frequency. The Q-factor is similarly controlled with a five-bit code. The Q range is from 0.57 to 150, and the break frequency range is 0.5 Hz to 25 kHz.

R5604, R5605, R5607 — Reticon

These are octave filters. All contain six-pole Chebyshev filters; however, they contain different numbers of filters with different pass band widths. The R5604 contains three 1/3 octave ANSI Class III filters that together cover an entire octave; the R5605 contains two ½ octave filters that together cover an octave, and the R5607 contains one full-octave ANSI Class II filter. The centre frequency of all the filters is controlled by the single clock input — see the response curves for details. The dynamic range is better than 80 dB and distortion is less than 0.1%. The filters can handle input signals greater than 10 V peak-to-peak and have an insertion loss of less than 0.2 dB in the pass band.

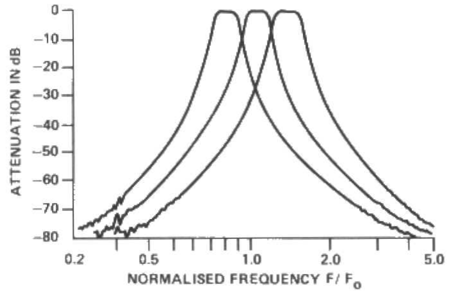
PIN	R5604 FUNCTION	R5605 FUNCTION	R5606 FUNCTION
1	V–	V–	V–
2	N/C	N/C	N/C
3	IN 2	IN 1	N/C
4	IN 1	N/C	N/C
5	V+	V+	V+
6	N/C	N/C	N/C
7	TRIG IN	TRIG IN	TRIG IN
8	N/C	N/C	IN 1
9	IN 3	IN 2	V–
10	V–	V–	N/C
11	N/C	N/C	N/C
12	V+	V+	V+
13	COM	COM	COM
14	OUT 3	OUT 2	N/C
15	OUT 2	N/C	N/C
16	OUT 1	OUT 1	OUT 1

(a) R5604

R5604 3-1/3 OCTAVE BAND-PASS FILTERS

f_{SAMPLE} = 55 kHz

F_o = 1 kHz

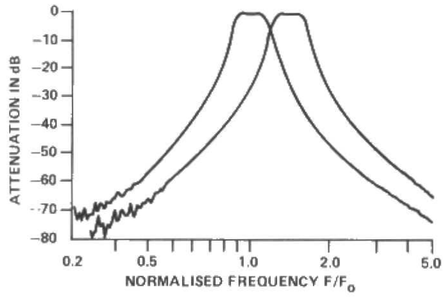


(b) R5605

R5605 2-½ OCTAVE BAND-PASS FILTERS

f_{SAMPLE} = 55 kHz

F_o = 1 kHz

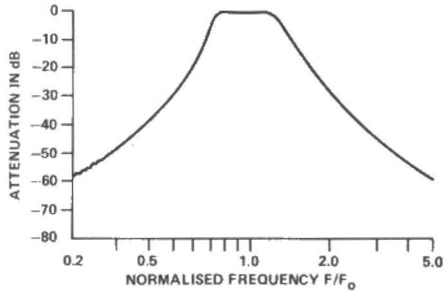


(c) R5606

R5606 1 FULL OCTAVE BAND-PASS FILTERS

f_{SAMPLE} = 55 kHz

F_o = 1 kHz



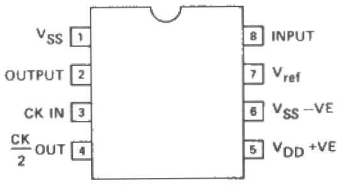
R5609, R5611, R5612 — Reticon

The R5609 is a seven-pole, six-zero elliptic low-pass filter with over 75 dB out-of-band rejection and less than 0.2 dB of pass band ripple.

The R5611 is a five-pole Chebyshev high-pass filter with 30 dB per octave rolloff and less than 0.6 dB of pass band ripple.

The R5612 is a four-pole notch filter with over 50 dB of rejection at the notch frequency.

The corner/center frequencies of these switched capacitor filters is tuneable by the input trigger frequency over a wide frequency range from 0.1 Hz up to 25 kHz. The dynamic range is better than 75 dB and distortion is less than 0.3%. Signal handling capability is over 12 V peak-to-peak, and typical insertion loss is 0 dB. Supply voltages may be ± 4 V to ± 11 V maximum.



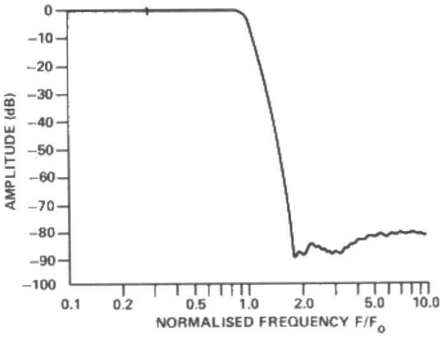
PIN OUT
(ALL 3 DEVICES)

SUPPLY VOLTAGE ± 4V TO ± 11V MAX.

(a)R5609

FREQUENCY RESPONSE OF R5609 LOW-PASS FILTER

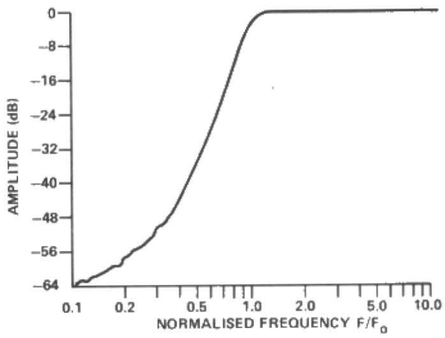
NOTE: f_c/F_o = 100 (typical)



(b) R5611

FREQUENCY RESPONSE OF R5611 HIGH-PASS FILTER

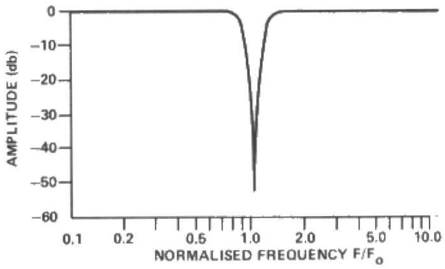
NOTE: f_c/F_o = 500 (typical)



(c) R5612

FREQUENCY RESPONSE OF R5612 NOTCH FILTER

NOTE: f_c/F_o = 930 (typical)



SPECTRUM ANALYST

Now that you've all finished the ETI Bargraph in the July '82 issue, we offer you the chance of a lifetime. Build our Spectrum Analyst and your TV set becomes a superb spectrum analyser. See your sound in your own home. Design and development by Phil Walker.

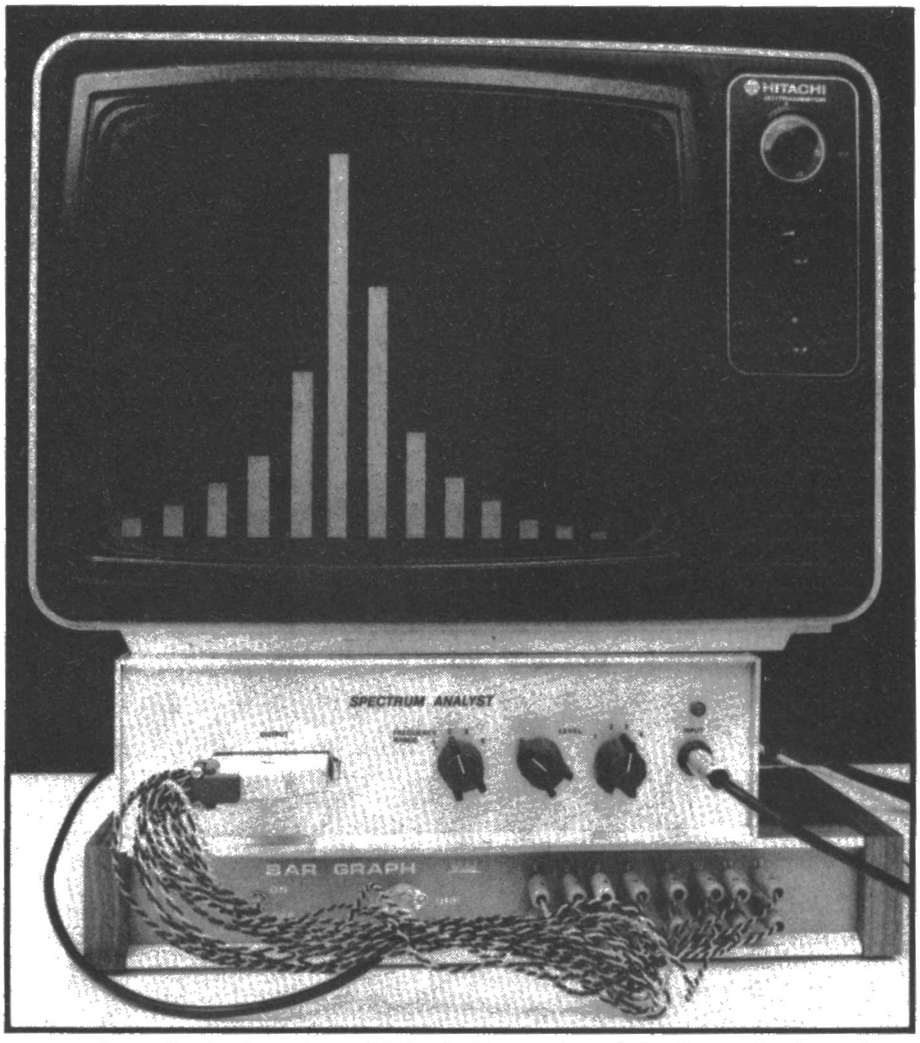
This project makes use of the recent introduction to the electronics armoury, the MF10 digital filter IC. With this device it is possible to construct filters whose passband frequencies are independent of passive components.

Here we use the MF10 in its band-pass mode. The centre frequency of the band is determined by the frequency of the clock signal supplied to it and is typically a hundredth of it. In order to cover as much as possible of the audio spectrum without incurring great expense, the basic instrument covers five octaves with 16 filters. The centre frequencies of the filters are spaced at approximately one-third of an octave. To extend the useful range of the instrument, the clock signals to the filters can be switched over three additional octaves, thus giving a total range of the eight octaves from 64 Hz to 16 kHz for the complete unit.

Coincidentally, the basic Bargraph unit is capable of simultaneously displaying the 16 channels output from the Spectrum Analyst.

New Chips For Old Jobs

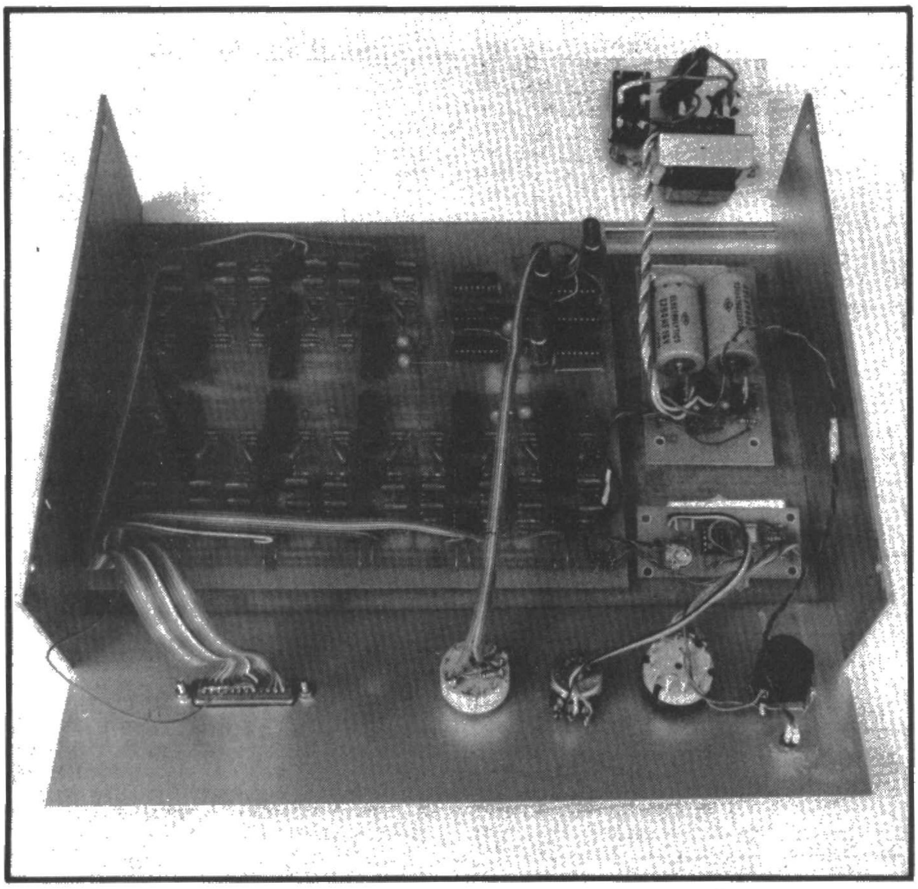
The MR10, recently introduced by National Semiconductor, contains within its 20-pin package two almost independent switched capacitor filters. Each section consists of an inverting mixing operational amplifier, a summing node internally switchable between ground or the low-pass output, and two switched capacitor integrators. These latter give band-pass and low-pass outputs. The output from the mixing op-amp is also made available. By various connection systems, the filter chip can be made to perform many of the jobs normally requiring a number of inductors, capacitors and resistors in passive configurations or several op-amps and other components in more conventional active circuits.



Here we have the Analyst plugged into the Bargraph and the Bargraph plugged into the TV, which is displaying the frequency spectrum of the audio input.

A feature that makes this device so much more useful than the other configurations mentioned above is that the frequency of operation can be determined externally by controlling the frequency of the clock signal applied to it. This means that without altering any component values, one filter can be tuned to a specific frequency very easily or can be changed to another frequency while retaining the same response shape.

The device is capable of simultaneously providing combinations of high, low and band-pass responses and a band-stop or notch response. In the many different modes of operation of the device not all of these responses are available simultaneously and some combinations of modes in the two filters in the same package are not possible; but in practice these limitations don't usually detract from the overall usefulness.



Here we've dismembered the Classic II case to show the internal layout. Note the resistors soldered to the pins of SW2; Fig. 8 refers. Ribbon cable is essential for a neat finish.

HOW IT WORKS

PREAMPLIFIER (FIG. 1)
The input goes via SW1 to the attenuator network R1 to 6 and then via C1 to the protection network D1, 2. It is then amplified by IC1a and passed to RV1 which acts as a variable attenuator. From RV1 the signal passes via C2 to IC1b where it is amplified by a factor of between 2 and 6 set by PR1. The output from IC1b is at a low impedance to drive the filter networks.

The Circuit

The circuit for this project is in four major parts: the input amplifier, the clock generator, the filter and rectifier units, and the power supply. The input amplifier provides signal level matching and buffering before driving the filter modules, and consists of a switched attenuator (SW1), followed by an inverting amplifier (IC1a), a variable attenuator (RV1) and a buffer with gain (IC1b).

The clock generator provides all the different clock frequencies to drive the filter ICs and set their operating centre frequencies. By means of SW2 and IC2a and IC2b, four sets of clock frequencies are made available. The sets of clock signals are in the ratio of 1, 2, 4, 8 to each other. This means that the operating band of the complete unit, itself covering five octaves, can be switched over four octaves giving a total coverage of eight. With the component values as shown the circuit covers the range of 64 Hz to 16 kHz but if a lower band is required then lower frequency crystals may be used (NB the input and interstage coupling capacitors may need to be increased in value.)

The next section is concerned with the filters and rectifiers themselves. These are configured around the MF10 digital filter IC. For this project the devices are used as band-pass filters with a Q-factor of about three. Their centre frequency is determined by the signal fed into them from the clock generator; the clock frequencies are at about one-third octave spacing from each other and the eight ICs provide a total of 16 filter channels covering five octaves altogether.

The filtered output from the MF10 devices then passes to a buffer which increases the drive capability and provides some gain before driving the rectifier circuit and output buffer. The rectifier circuit has a fairly slow time constant of about one second to make the display steady. For a time constant nearer the accepted standard for VU meters, change all the 10M resistors (R117-132) to 3M3 instead.

The final circuit section is the power supply. This is quite straightforward and consists of a centre-tapped transformer feeding a bridge rectifier and reservoir capacitors. The unsmoothed DC on the capacitors is then regulated by four IC regulators to give the four supply rails needed by this project. On the main board there are several extra capacitors across the supply rails whose purpose is to suppress noise and possible instability which might affect the operation of the circuitry. Note the use of ceramic (not polyester) capacitors for C76 and 77 — these components require a low inductance.

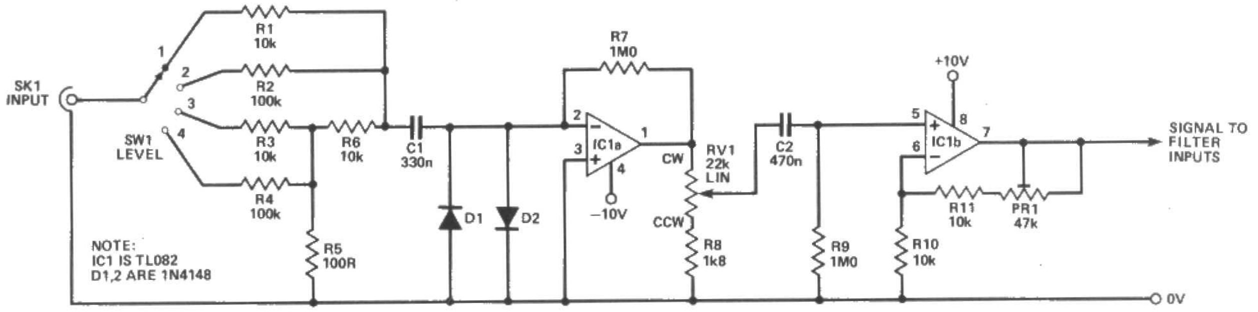


Fig. 1 Circuit diagram of the input preamplifier.

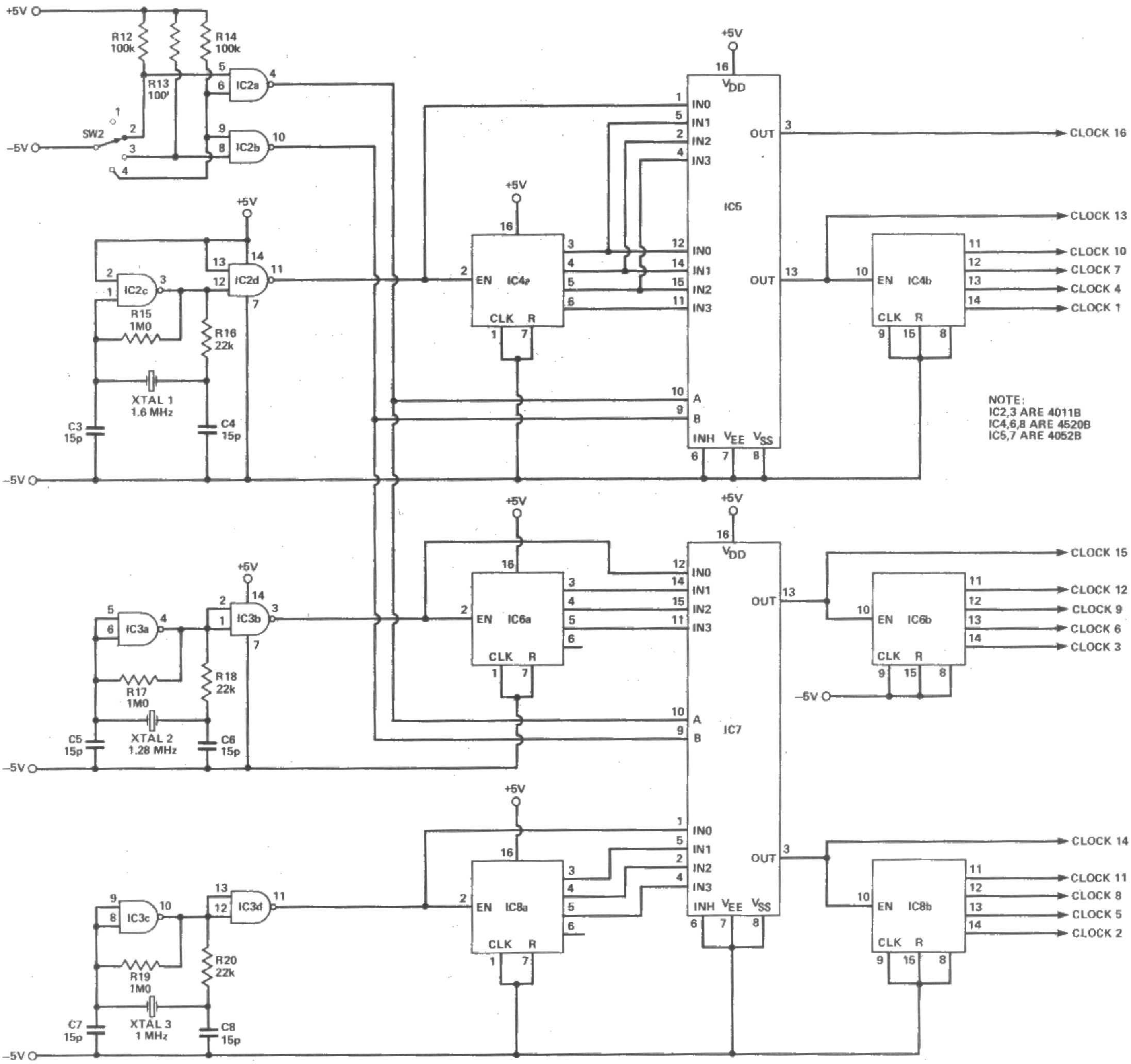


Fig. 2 Circuit diagram of the clock generator. The filter centre frequencies are determined solely by the frequencies CLOCK 1–CLOCK 16.

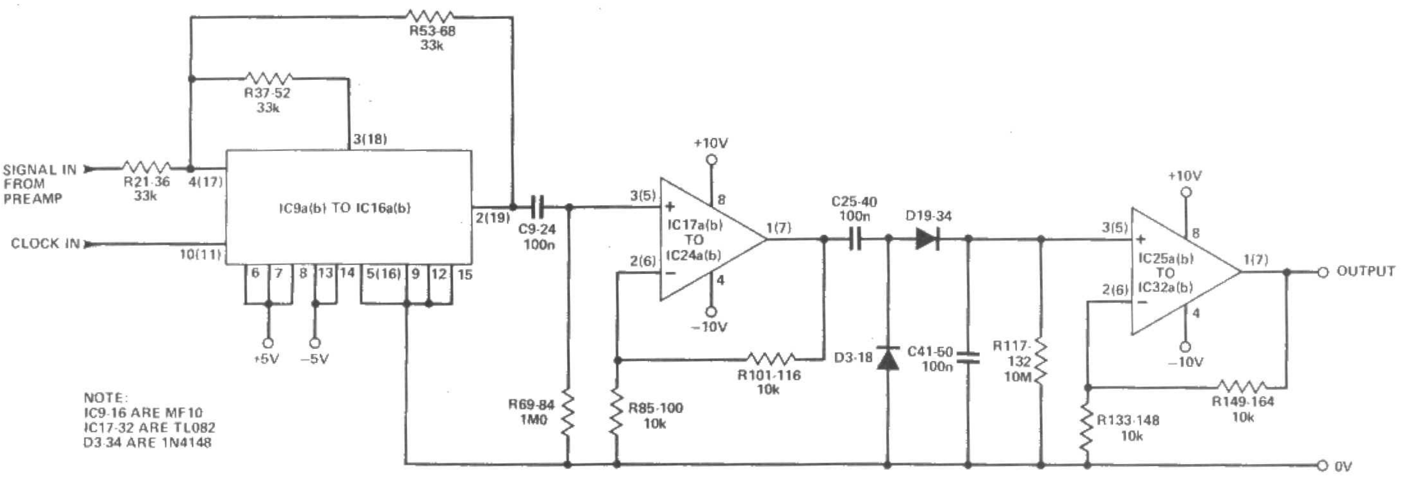


Fig. 3 Circuit diagram of one filter-rectifier block. There are a total of 16 similar blocks, each driven by a different output of Fig. 2.

HOW IT WORKS

CLOCK GENERATOR (FIG. 2)

There are three high frequency clock generators in the project, all of which operate in the same way; we'll look at the operation of the first one. IC2c is biased by R15 so that it would normally be near the centre of its transfer characteristic; its output is taken, via a low-pass filter (R16/C4) to discourage spurious oscillation modes, to a quartz crystal XTAL1. The other end of the crystal connects to the input of IC2c and another small value capacitor. The characteristic of a crystal such as the one used here is that it behaves like a very high Q tuned circuit. This means that not only does its impedance change very rapidly near its resonant frequency but also its phase response. At some frequency very close to the resonant frequency then, the feedback from output to input of IC2c wil be of the correct phase and magnitude to cause it to oscillate. Moreover the frequency will be determined almost completely by the mechanical characteristic of the crystal so that the frequencies eventually output are very accurately controlled. The output from IC2c is connected to IC2d which acts as a buffer for the oscillator output and also improves the wave shape.

The output from IC2d is taken to IC4a (half a 4520) which is a four bit counter/divider. This gives four outputs each half the frequency of the preceding output. One of these outputs is selected by one channel of IC5, a dual one-of-four selector, and passed to IC4b.

IC4b provides four outputs; again, each a factor of two slower than the one before. These, together with the output from IC5 pin 13 give five of the six clock outputs required for this part of the circuit. The remaining signal is selected by the other channel of IC5 from the three faster outputs from IC4a (pins 3, 4, and 5) and the output from IC2d. The net result of all this switching is that six outputs are obtained, each of which is half or double the frequency of its neighbours.

The remaining two clock generators are very similar in operation but rather simpler in circuitry as only five outputs are required from each of them.

The two dual one-of-four selectors used in the three clock generators determine which of four frequency bands the instrument will operate upon. The select inputs to these devices are driven by IC2a and IC2b. These are connected such that they convert the position of SW2 into a two bit digital code which then addresses the selector chips IC5 and 7 to provide the correct clock speeds.

FILTERS AND RECTIFIERS (FIG. 3)

There are 16 identical filter blocks, only one of which is illustrated in Fig. 3. The outputs from the clock generators each drive half of a filter IC type MF10; thus the only difference between channels is the clock frequency. These devices are connected to operate as band-pass filters with a Q of about three; their overall mid-band gain is set to unity. The centre frequency of the pass-band is determined by the clock frequency fed in to that half of the filter chip. (For more information see Designer's Notebook elsewhere in this issue.) In this design it is one hundredth of the clock frequency. The output from the filter passes to an amplifying buffer (IC17a etc) and then to a charge pump rectifier composed of C25, C41, D3, D19 and R117.

The resulting voltage on C41 is then amplified by IC25a and passed to the output terminal. R117 acts both as a DC bias path for the buffer amplifier input and as a discharge path for the rectifier output capacitor.

POWER SUPPLY (FIG. 4)

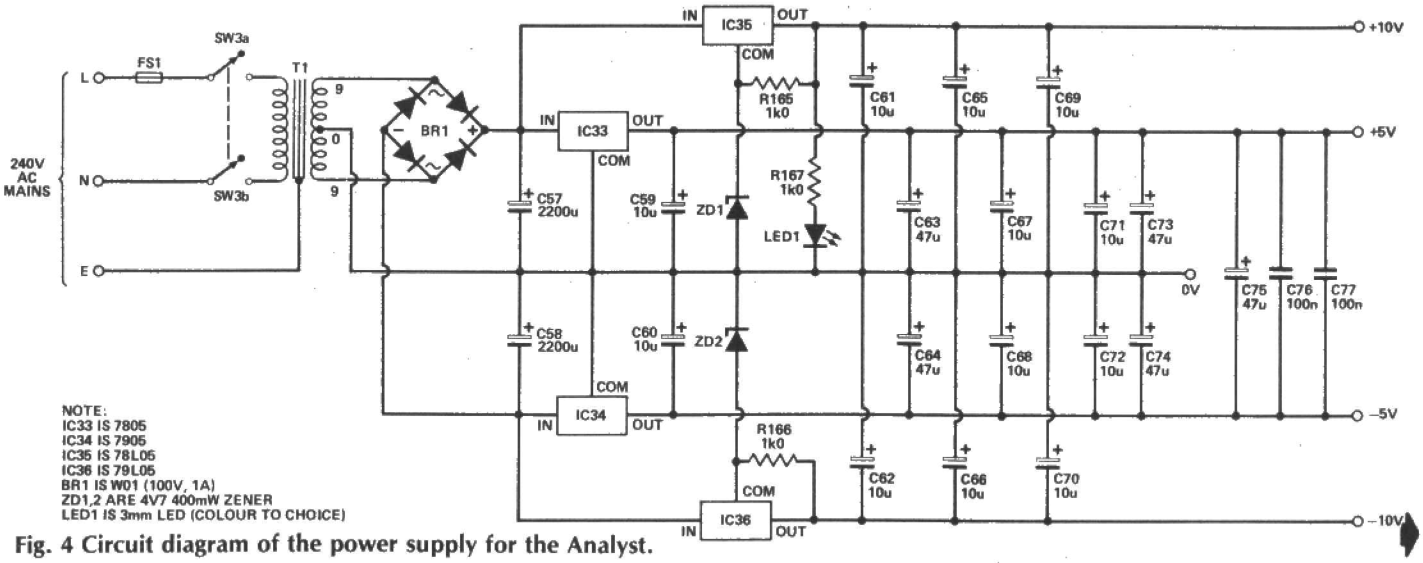
This is very simple and straightforward consisting of a centre tapped transformer, bridge rectifier, filter capacitors and four monolithic regulators. Zener diodes in the common leads of the +10 and —10 V regulators are used to boost their voltage from their normal 5 V, as 10 V devices are not usually obtainable. The +10 and —10 V rails are provided for the op-amps and the rectifier circuitry while +5 and —5 V has to be supplied to the filter chips. The latter supplies also power the CMOS logic devices. This is convenient as it also removes any doubt about clock drive levels to the filter chips. The remaining capacitors on the supply lines are fitted to reduce the possibility of noise and glitches getting into the circuitry. It is possible that some capacitors could be left out without undue effect but this cannot be guaranteed.

Construction

The construction of this project is fairly simple so long as care is taken with soldering, especially around the clock generator circuitry. We recommend the use of sockets for all the ICs and especially the MF10s as these are quite expensive. (NB this does not apply to the regulator ICs).

When assembling the PCBs do not forget to insert the wire links where shown. There are two connections to be made between the 4052s; make sure you don't get your wires crossed. Check all the components carefully as you put them in to make sure you get them the right way round. Some of the small capacitors have been provided with alternative lead holes on the PCB so don't be worried by the occasional unfilled hole; this is a public service for readers with odd-shaped capacitors! It is advisable to bend the crystal wires gently before inserting them into the board so that you can get to the ICs next to them. R12, 13, 14 are mounted on the back of SW2 using any spare terminal; Fig. 8 shows how we do it. The mains components are mounted on the back panel well away from the input amplifier. The indicator LED1 is mounted on the front panel with flying leads to the power supply board. We found that using ribbon cable for most of the main board to front panel connections made a much neater job, as the photographs show.

There are many ways to connect the Analyst to the Bargraph and the one we used here was a 'D' range connector. This is a little on the expensive side but makes a very neat job. It is quite possible to use these connectors on the Bargraph



NOTE:
IC33 IS 7805
IC34 IS 7905
IC35 IS 78L05
IC36 IS 79L05
BR1 IS W01 (100V, 1A)
ZD1,2 ARE 4V7 400mW ZENER
LED1 IS 3mm LED (COLOUR TO CHOICE)

Fig. 4 Circuit diagram of the power supply for the Analyst.

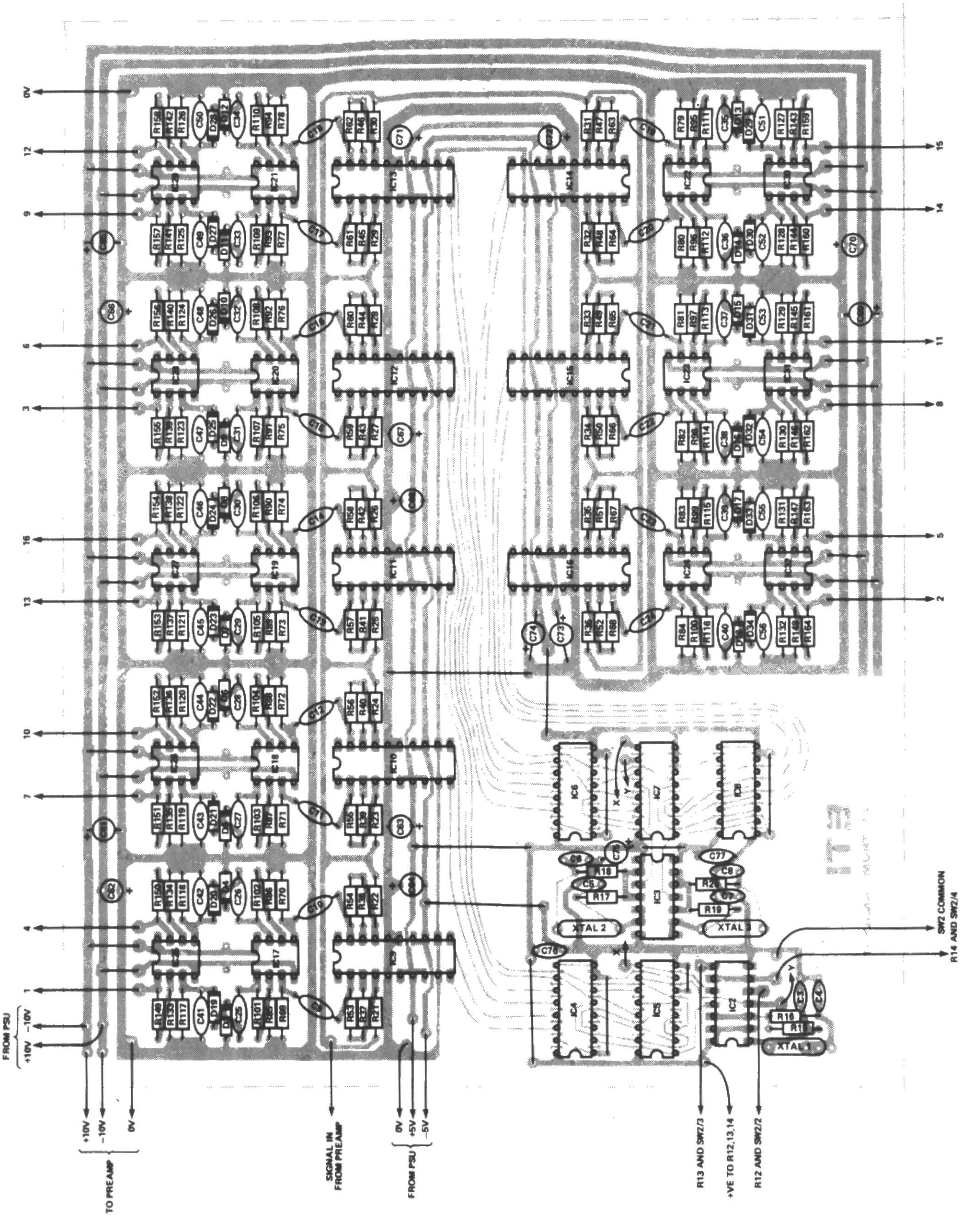


Fig. 5 Component overlay for the main filter board of the Spectrum Analyst. The spare holes between the op-amps (eg IC17 and IC25) are for additional 100n decoupling capacitors, should you find this necessary.

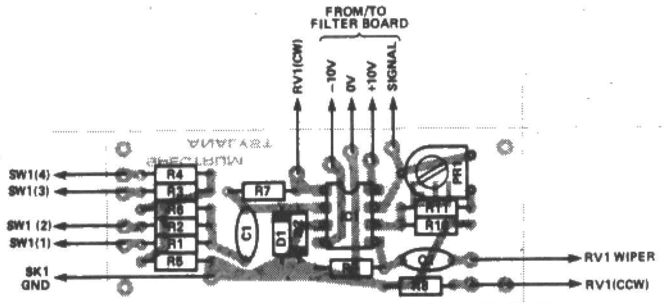


Fig. 6 Component overlay for the preamplifier board.

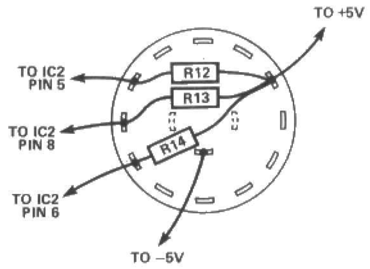


Fig. 8 Details of SW2.

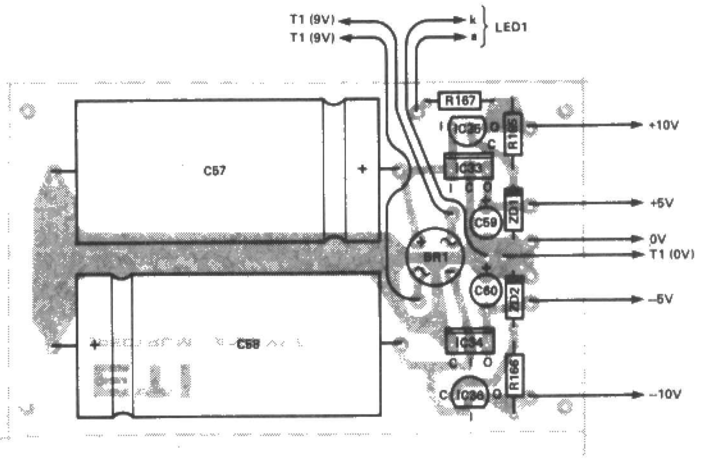


Fig. 7 Component overlay for the PSU board. Heatsinks are not required on the IC voltage regulators.

as well if you have not already made it. Naturally it is also quite simple to use the same sort of jack sockets on the Analyst and thus possibly save a little money in the process. The choice is entirely yours.

Operation

Using this device is very simple. The outputs from it are plugged into the Bargraph display unit, an audio signal is plugged into the Analyst and the front panel controls adjusted for a good display.

BUYLINES

Being a fairly new chip, the MF10 is likely to be a bit thin on the ground. However, the IC is being stocked by Rapid Electronics, Hill Farm Industrial Estate, Boxted, Colchester, Essex CO4 4RD; the price is £2.50 per chip. The three crystals for this project can be obtained from Watford Electronics, while Watford or Cricklewood Electronics can supply the D-Range connectors. The PCBs can be obtained from our PCB Service using the order form on page 91, while West Hyde, suppliers of the case we used, are at Unit 9, Park Street Industrial Estate, Aylesbury, Bucks.

In order to get the best out of the Bargraph display it is necessary to insert R13 on the main board in order to change the reference voltage. A value of 33k should be a good starting point; the effect of this is to lower the 0 V reference level on the display towards the bottom of the screen. As the output from the Analyst is only positive-going the negative part would waste half the screen area.

The outputs from the main board of the Analyst are numbered 1 to 16. Output 1 corresponds to the highest frequency band. To get the normal type of display, output 1 from the Analyst should go to input 1 of the channel card nearest to the main board of the Bargraph. The channels should then follow on from there.

If you do not want to use the Bargraph display you will need some means of displaying 16 channels of varying DC levels in the range of about 0 to 10 V maximum. This is no easy or cheap feat, and, though there are several ways of doing it, they will probably work out more expensive than the Bargraph.

PARTS LIST

Resistors (all ¼W, 5%)	
R1,3,6,10,11,37-52, 85-116,133-164	**10k**
R2,4,12-14	**100k**
R5	**100R**
R7,9,15,17,19, 69-84	**1M0**
R8	**1k8**
R16,18,20	**22k**
R21-36, 53-68	**33k**
R117-132	**10M**
R165-167	**1k0**
Potentiometers	
RV1	**22k linear**
PR1	**47k miniature horizontal preset**
Capacitors	
C1	**330n polycarbonate**
C2	**470n polycarbonate**
C3-8	**15p ceramic**
C9-56	**100n polyester**
C57,58	**2200u 16 V axial electrolytic**
C59-62,65-72	**10u 25 V tantalum or PCB electrolytic**
C63,64,73-75	**47u 16 V tantalum or PCB electrolytic**
C76,77	**100n ceramic**
Semiconductors	
IC1,17-32	**TL082**
IC2,3	**4011B**
IC4,6,8	**4520B**
IC5,7	**4052B**
IC9-16	**MF10 (see Buylines)**
IC33	**7805**
IC34	**7905**
IC35	**78L05**
IC36	**79L05**
D1-34	**1N4148**
ZD1,2	**4V7 400 mW zener diode**
BR1	**W01 (100 V, 1 A)**
LED1	**3mm green LED or similar**
Miscellaneous	
XTAL1	**1.6 MHz crystal**
XTAL2	**1.28 MHz crystal**
XTAL3	**1.0 MHz crystal**
SW1, 2	**1-pole 4-way rotary switch**
SW3	**2-pole mains-rated toggle switch**
T1	**9-0-9 6 VA mains transformer**
FS1	**500 mA 20 mm fuse and holder**
SK1	**¼" jack socket**
SK2	**25-way 'D-Range' plug, socket and cover**

PCBs (see Buylines); three knobs; case to suit (West Hyde Classic II code BEL); grommets, wire, sleeving etc; 16 off 2.5 mm jack plugs to connect with Bargraph.

ETI

DESIGNING MICRO SYSTEMS PART 4

In this article Owen Bishop examines RAM. If you seek enlightenment about horned ruminants, however, read no further.

Strictly speaking, random access memory (or RAM, for short) includes every part of a computer's memory which can be read to obtain information and can be written into to store information. In other words, everything that is not ROM (read-only memory — see last month's article) is RAM. This RAM includes not only the arrays of ICs in which information is stored by solid-state circuitry, but also any magnetic cassette tape-recorder or disc drive which may be connected to the micro. Tape-recorders and disc drives will be considered in Part 7 of this series, because, both in form and in function, they are entirely different from the solid-state devices on the computer board. Most people nowadays take the term RAM to cover only the ICs and not the magnetic storage devices.

The name 'random access memory' is a curious one and something of a misnomer. 'Random access' means that the computer can go instantly to any memory cell (a bit) or any group of eight memory cells (a byte) and read from it or write into it. The computer can skip from one location to another according to the program. The situation is analogous to the **random access file,** used in data base systems, and usually stored on disc or tape. The computer can find any location within the file almost instantly and read from it or write to it, without affecting the adjacent locations. This contrasts with the **serial access file,** in which every location in the file must be read from or written into in order, from the beginning of the file to the end.

While the use of the term 'random access' (as opposed to 'serial access') is fairly clear in connection with tiles, even so, it is unlikely that the computer would be accessing items in the file purely on a chance or *random* basis. it usually has a very precise notion of which location it should access on any one occasion. The term 'random access' is even more unsuitable in connection with memory. The computer can, and frequently does, skip about from one part of *ROM* to another, particularly if there is a BASIC interpreter in ROM and it has to go to a different section of ROM to process each command. So ROM is accessed in the same fashion as RAM, and the term RAM makes an inapplicable distinction. A better pair of terms would be ROM (read-only memory) and RAWM (read and write memory), but it seems that we are saddled with RAM and must continue to use it despite its illogicality. A strange anomaly in the world of logical machines!

Where Do You Use RAM . . .

The essence of RAM is that it is *alterable*. You can store information in it, alter parts of the information if required, or replace it altogether with an entirely new lot of information. Some of the main uses of RAM in a micro are:

Scratch-pad This is a (usually) small area of memory reserved for holding information about the state of the system, or where the computer 'jots down' the intermediate results of a series of calculations, ready to be picked up again at some later stage. The scratch-pad can hold such information as the address where the table of variables begins. This is called a **pointer** to the variable table. There wil also be a pointer to the location of the first line of the stored BASIC program, and to other important locations in RAM.

Some locations in the scratch-pad may hold parameters connected with the operation of the system, such as the positions of the margins of the graphics display areas on the monitor screen, the current screen position of the cursor (that small flashing rectangle which moves around the screen as you type), or the name of the key most recently pressed. There may also be 'flags', which are bytes that indicate certain states of the system. For example, INVFLG at address 0032 in the Apple holds the value −1 if the screen is to display normal text, 0 for flashing text and +1 for inverse text.

In 6502-based micros, such as the BBC Microcomputer and Apple, the scratch-pad is usually located at the bottom of memory (the early addresses 0000 to 00FF). This allows the monitor to take advantage of the faster and simpler zero-page addressing featured by the 6502, as mentioned last month. In other micros the scratch-pad may be at the bottom *or* top, but is usually not in the middle, where it could so easily be overwritten by loaded programs.

Tables of variables This may include arrays and strings, for use in the program.

The program itself This may be in BASIC or some other high-level language, or in machine code. Often small machine-code programs (such as editing or renumbering programs) can be tucked away at one end of RAM, where they will not be disturbed by the main program.

The video RAM This is an area of RAM set aside for holding information about what is to be displayed on the screen. The video RAM is usually near the lower end of memory, perhaps just above the scratch-pad. More about this in Part 5.

Buffer RAM These are sections of memory reserved for holding data temporarily before it is transferred somewhere else. For example, when you type in a line of program, your keystrokes are stored in a **line buffer.** When you press 'Return' or 'Enter' the line you have just typed is tranferred from the buffer to the next vacant locations in the area where the program is being stored. Buffers are useful when data is to be transferred rapidly between the micro and a peripheral device such as a printer or disk drive. A block of incoming information, such as the contents of a file on disc, are held in a file buffer in RAM. It is then available for use by the main program, and can be replaced by information from other files in due course.

. . . And How Much Do You Need?

The amount of RAM a system requires depends on how many of the functions listed above are to be implemented. A microprocessor control system (such as that fitted in an automatic washing-machine) will have its program in ROM (or PROM). The washing machine has no video, and needs no variable table or RAM buffers, but it may need a scratch-pad on which to keep account of the settings of the controls or the stage it has reached in processing the washing. It needs a very small RAM, simply as a scratch-pad. An IC such as the Mostek MK3805 (Fig. 1) provides just 24 bytes of RAM. The chip also includes a real-time clock-calendar.

At the other extreme many personal computers come with between 16K and 48K of RAM, and can be expanded up to 64K or even more. The great advantage of this is that lengthy programs can be loaded, making it possible for the computer to run anything from a sophisticated accounts program to a complex and perplexing adventure game. It is the steady decline in the cost of RAM ICs which has led to the increasing power and hence increasing popularity of the personal microcomputer. Nowadays the typical micro has enough RAM to do things which formerly only an expensive mini could do. In 1974, the only RAM ICs available on the hobby market were the TTL 7481 and 7489. The 7489 cost £4.95, and contained 64 bits (16 four-bit words), a rate of 13 bits per pound. In spite of inflation we can today buy a 64 *kilobyte* IC for only £13.40, a rate of about 4000 bits per pound.

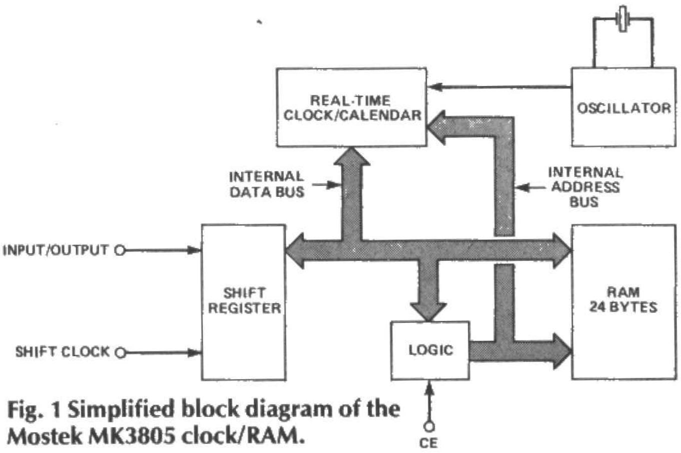


Fig. 1 Simplified block diagram of the Mostek MK3805 clock/RAM.

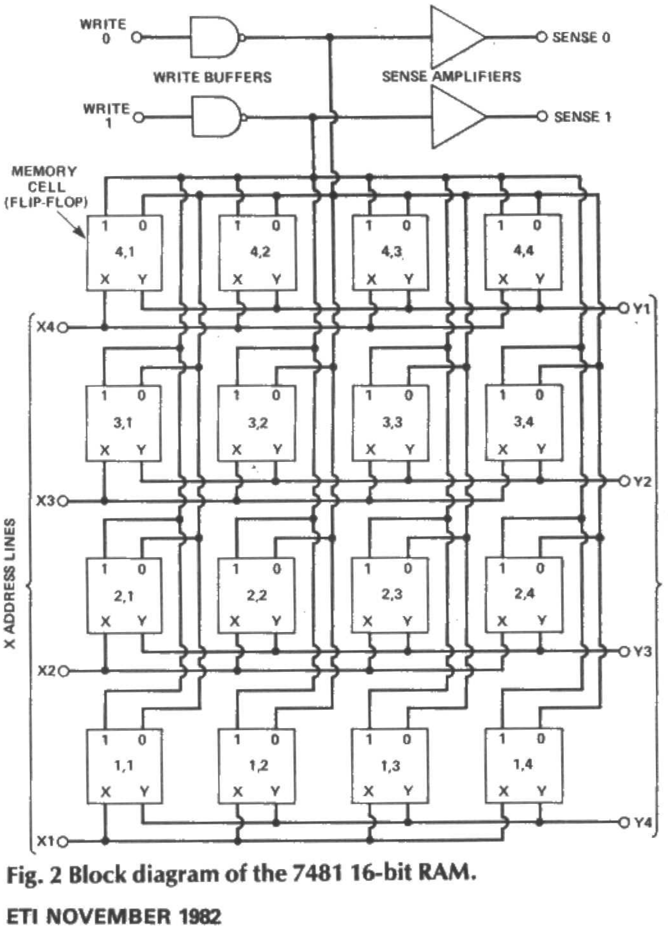


Fig. 2 Block diagram of the 7481 16-bit RAM.

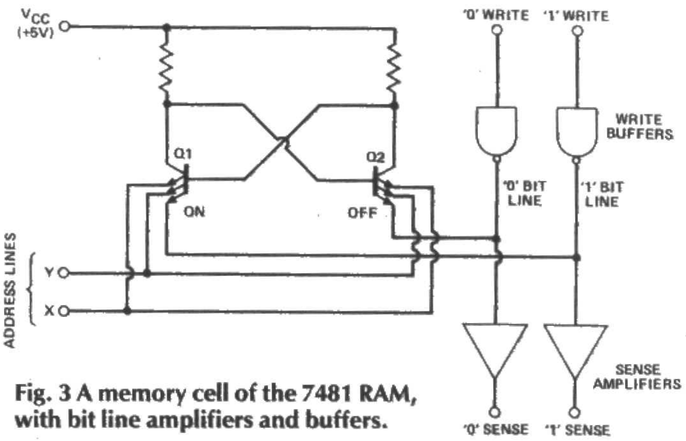


Fig. 3 A memory cell of the 7481 RAM, with bit line amplifiers and buffers.

Bipolar Bistables = Bits

The 7481 and 7489 are early examples of RAM based on bipolar transistors. The 7481 (Fig. 2) has 16 bits, each individually addressable. Each bit is represented by a flip-flop (Fig. 3). Readers will recognise the familiar cross-connected configuration of the transistors, but the triple emitters are a distinctive feature.

Each flip-flop can be in one of two states, one of which represents a stored '0' and the other a stored '1'. In Fig. 3 the flip-flop represents '1' when Q1 is on and '0' when Q1 is off. The address lines X and Y are normally low, and the current through the 'on' transistor (Q1 in this example) flows to the address lines. To address any particular flip-flop the corresponding lines for row and column are made high. The result of this is that for the addressed flip flop, both X and Y lines become high. For the other flip-flops at least one of X and Y is low.

Let us follow the way the stored data is read from the flip-flop. Figure 4 shows what happens. When both address lines go high, the current (if any) through the transistor can no longer flow to the address lines. Instead it is diverted to the bit line, in this example the '1' bit line. The current is detected by the sense amplifier, the output of which falls from its normal state ('1') to '0'. No current is flowing through Q2, so the '0' bit line and its amplifier are unaffected. It needs only a logic gate and buffer to output the signal from the sense amplifiers to the data bus of the computer. Reading has no effect on the contents of the flip-flop. Q1 stays on due to the current flowing to the '1' bit line. Q2 is off and stays off.

Now let us look at the write operation (Fig. 5). Inputs to the write buffers are normally low. To write a '0' at the flip-flop we apply a 'high' voltage to the '0' write buffer and make the appropriate address lines high. The buffers are inverters, so their output is not normally '0'. Now the output on the '0' bit line changes to '0'. Q2 is able to conduct because of the low level on the '0' bit line. Consequently the flip-flop changes state, the stored '1' being replaced by a '0'. Had we tried to write a '1' to this flip-flop, the flip-flop would have remained in its previous state.

Figure 6 shows another way in which bipolar transistors may be used in RAM. There is only one address line, common to four or more flip-flops holding the data of one nibble (four bits) or one byte. Apart from this, the operation is very similar to that of the flip-flop described above.

A Static RAM Gathers MOS

The use of MOS transistors allows more flip-flops to be packed on to the chip, thus making the building of really large memory arrays much simpler and cheaper. Just as important is the fact that MOS has much lower power requirements than bipolar circuitry. One transistor of each bipolar flip-flop is always in the conducting state, so even a small RAM IC continuously draws a current that is tens of milliamps. Supplying current to a large bipolar RAM and dissipating the heat generated are major problems. Nevertheless bipolar RAM has the advantage of very high speed of access (of the order of 20 nanoseconds). It is favoured in input and output buffers of main-frame computers where large amounts of data have to be transferred at high speed between the computer and peripherals such as hard-disc drives.

By contrast, MOS circuits require hardly any current while in the quiescent state. The 5101 CMOS RAM (Fig. 7) draws only 10 uA while quiescent. Even when it is being read from or written into at maximum rate, the current requirement never exceeeds 25 mA. The price for low current consumption is paid in longer access times — of the order of 450 nanoseconds — though some MOS RAMs are faster. However, longer access time is no disadvantage for the typical micro.

Figure 8 shows a typical MOS memory cell. It has the same general structure and connections as its bipolar counterpart, except that it employs two transistors (Q3, Q4) to act as drain resistors. These are easier to fabricate on the chip than ordinary resistors would be.

One of the distinguishing features of solid-state RAM is that it loses all stored information when the power is switched off. Provided that the power supply to the micro has provision for covering brief interruptions of the mains supply, this is not a problem. In portable computers which are to be used in the field, and in pocket calculators, it may be desirable that stored information should be retained while the power is off. To retain the information in RAM, some kind of battery back-up is needed for the RAM section of the computer circuit, though power to the display and peripherals can be completely shut off. Here again, MOS circuitry has its advantage of microamp power consumption in the quiescent state (ie when not being used). A small battery retains information in memory for weeks or months. The 5101 has the additional feature of requiring only a 2 V supply to retain memory, though it normally operates on 5 V.

A Wee DRAM? It's Refreshing

The devices described above all belong to the class known as static RAM. Once a flip-flop has been set to a given state, it remains in that state until the power is removed. It is **static.**

Modern micros also employ an entirely different type of RAM called **dynamic** RAM. The characteristic of this is that a memory cell does not hold its information indefinitely. After a while (a few microseconds) the stored information fades away. If information is to be retained, it must be renewed or 'refreshed' periodically.

Figure 9 shows the circuit of a typical memory cell. Eight such cells are connected to a single address line, which is normally held low (0 V). The eight cells hold the eight bits which make up a single byte of information. Decoding logic within the IC ensures that the address line goes high (+5 V) when the address of the byte, of which

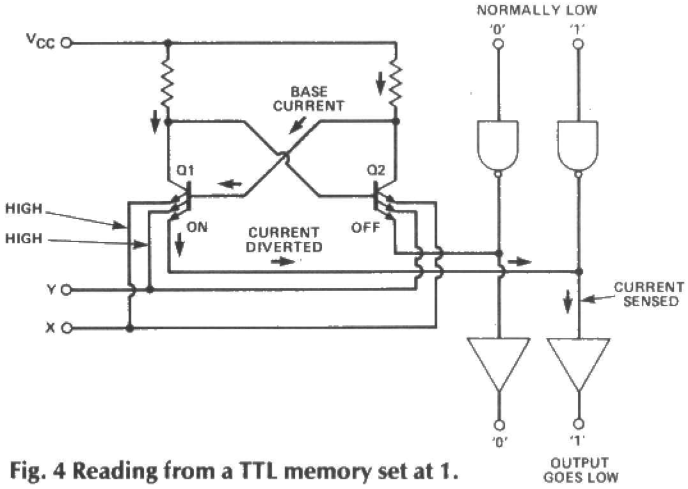


Fig. 4 Reading from a TTL memory set at 1.

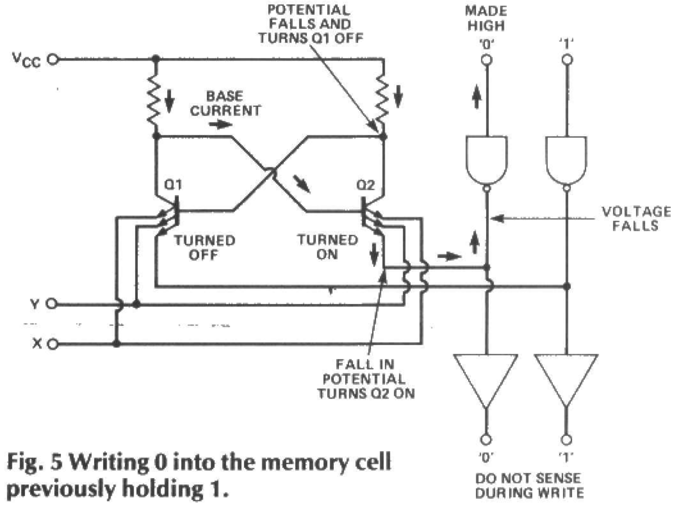

POTENTIAL FALLS AND TURNS Q1 OFF
MADE HIGH
'0'
'1'
VCC
BASE CURRENT
Q1
Q2
TURNED OFF
TURNED ON
VOLTAGE FALLS
Y
X
FALL IN POTENTIAL TURNS Q2 ON
'0'
'1'
DO NOT SENSE DURING WRITE

Fig. 5 Writing 0 into the memory cell previously holding 1.

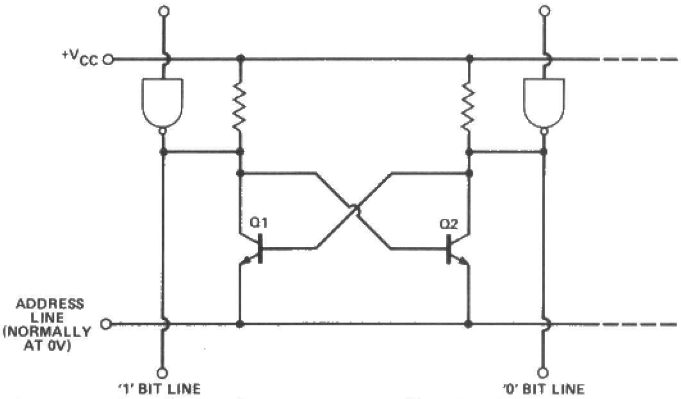


Fig. 6 Another design for a memory cell, using bipolar transistors.

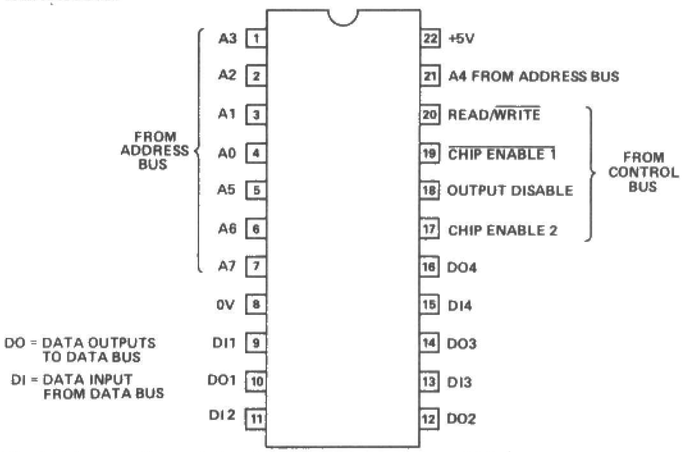


Fig. 7 Pin outline of the 5101 CMOS static RAM.

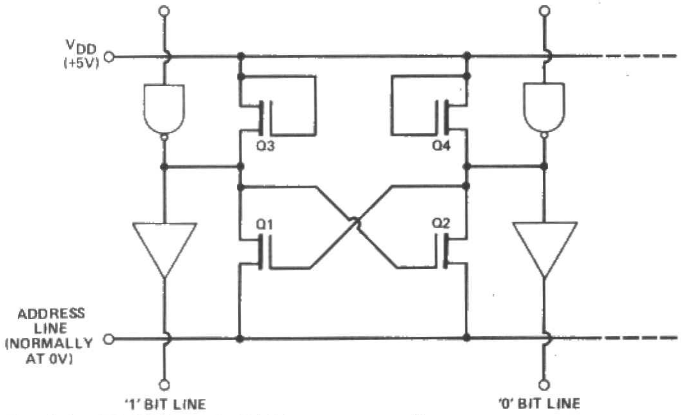


Fig. 8 An NMOS static RAM memory cell.

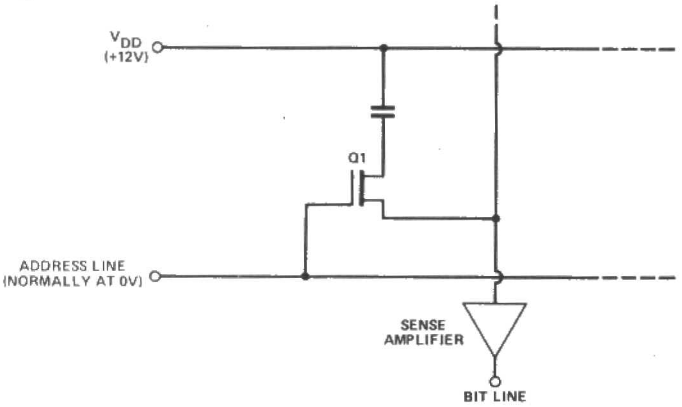


Fig. 9 A MOS dynamic RAM memory cell.

this cell is a part, is present on the address bus of the computer. Each of the eight cells is connected to a different bit line, one corresponding to each line of the data bus. Note that there is only a single bit line, not a '0' bit line and a '1' bit line.

When data is to be written into the cell, the address line goes high, turning on the transistor. If the bit line connected to that transistor is at 0 V, a potential difference of 12 V develops across the capacitor. If the bit line is at 5 V, the potential difference is only 7 V. The address line then goes low again and the potential across the capacitor remains. The effect of this operation is that the information is now stored on the capacitor. The information can be altered by making the address line high, with a different level present on the bit line.

The information can be read by making the address line high, once more connecting the capacitor to the bit line. Charge present on the capacitor is shared with a sense amplifier connected to the bit line. The amplifier outputs a '1' or '0' to the corresponding line of the data bus.

Left to itself, the capacitor would gradually lose its charge through leakage. It also loses some of its charge every time it is read. Figure 10 shows how the charge is refreshed. The 'switches' are in fact transistors in the control circuits of the IC. When both switches are set to position B they feed back the output of the sense amplifier to the bit line. This is positive feedback so the amplified output instantly restores the charge to its correct value.

The need to refresh RAM every few milliseconds imposes an additional task on the MPU, but the advantages of dynamic RAM (see later) are such that this is acceptable for a system with *large* amounts of RAM. Some microprocessors, such as the Z80, provide a special $\overline{\text{RFSH}}$ output which goes low during the second half of each of code fetch cycle. During the first half of this cycle the MPU reads an instruction from ROM or RAM. During the second half of the cycle it is busily processing the instruction internally before acting upon it. This is then a suitable time for the RAM to be refreshed. The $\overline{\text{RFSH}}$ signal, in conjunction with the $\overline{\text{MREQ}}$ (memory request, which also goes low while $\overline{\text{RFSH}}$ is low) can be used in various ways to instruct the RAM ICs to refresh themselves. To see how this is done, let us look at a commonly used dynamic RAM (or DRAM), the 4116.

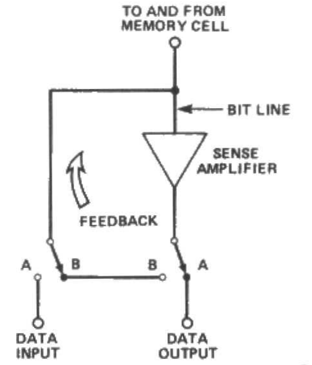


Fig. 10 Dynamic RAM control switching, shown set for data output, Feedback applies when both switches are set to B.

Dynamic RAM Gives Denser Data

This IC well illustrates the great advantage of dynamic RAM. The cells have so few components (compare Figs. 8 and 9) that they can be densely packed on the chip, giving us enormous numbers of cells in a single IC at relatively low cost. The 4116 (Fig. 11) is only a 16-pin device yet it can hold 16 kilobits of information. These are organised as 16K individually addressable bits. In practice we would take eight such ICs and operate them in parallel to obtain 16 kilo*bytes* of memory, one IC corresponding to each bit in the byte (Fig. 12).

A 16K RAM can cover addresses from 0000 to 3FFF (in hexadecimal); in binary this is from 00 0000 0000 0000 to 11 1111 1111 1111.

This means that 14 address lines are required to specify an address. A quick check of Fig. 11 reveals that the 4116 has only seven address input pins! Of course, if the IC had to have 14 address pins, it would need 23 pins altogether, making it physically much larger. We are up against one of the limiting factors with integration. No matter how much circuitry we can cram on to a chip measuring only a few millimetres across, connections to the world outside *must* be relatively large and relatively widely spaced. The case and the pins take up far more board space that the actual chip. Having larger ICs means that we can accommodate correspondingly fewer of them on the computer board, so throwing away some of the advantage gained by high-denisty packing on the chip. The use of seven address pins instead of 14 keeps IC size down yet requires only a little additional logic in the addressing system.

The addressing system is controlled by three signals (Fig. 13); $\overline{\text{RAS}}$ (row address strobe), $\overline{\text{CAS}}$ (column address strobe), and $\overline{\text{MUX}}$ (multiplex). These are obtained from the $\overline{\text{RFSH}}$ (if available), $\overline{\text{MREQ}}$, $\overline{\text{RD}}$ or $\overline{\text{WR}}$ outputs of the MPU in various ways by a simple logic circuit. In a 16K RAM there is only one row and one column, and $\overline{\text{RAS}}$ is identical to $\overline{\text{MREQ}}$. It goes low whenever a read or write operation is in progress. When $\overline{\text{RAS}}$ goes low the multiplexer (controlled by $\overline{\text{MUX}}$) already has the lines A0 to A6 connected to the RAM ICs. The low half of the required address is thus loaded into each IC. Remember that we are trying to load the same address into each of the eight ICs so as to access the eight bits corresponding to the same byte.

Next $\overline{\text{MUX}}$ goes high. This switches the multiplexer IC so that the RAM ICs are now connected to lines A7 to A13. An instant later $\overline{\text{CAS}}$ goes low and the upper seven bits of the address are loaded into each IC. The RAM ICs now hold the complete address and, after a short delay, the appropriate bit can be read or written in the usual way.

In a larger RAM we may have two or more sets (columns) of eight ICs, each with its own $\overline{\mathrm{CAS}}$ line. The appropriate $\overline{\mathrm{CAS}}$ line is selected by decoding the two upper address lines (A14 and A15) and combining them with the $\overline{\mathrm{CAS}}$ signal from the MPU. Columns which are not being addressed will receive and store the lower seven bits of any address as a result of the $\overline{\mathrm{RAS}}$ signal which all ICs receive. Only the addressed column will receive a $\overline{\mathrm{CAS}}$ signal and respond to a read or write operation. For other configurations of memory, it may be necessary to have several $\overline{\mathrm{RAS}}$ and $\overline{\mathrm{CAS}}$ lines to bring different memory blocks into operation by row and by column.

The $\overline{\mathrm{RAS}}$ input to the 4116 has an additional function, that of refreshing RAM. When $\overline{\mathrm{RAS}}$ goes low, the internal switches are thrown so as to refresh every cell in the IC. Thus during every read or write operation to RAM *all* ICs are refreshed while the low half of the address is being loaded. The $\overline{\mathrm{RAS}}$ signal operates for *all* read and write operations, whether these are to RAM or ROM. Thus, even while the MPU is reading a program from its monitor or resident language in ROM, is it still causing its RAM to be refreshed regularly.

One-Chip RAM

The majority of current micros have a 16-bit address bus and are therefore able to address up to 64K. This must include ROM too, so it would be uneconomical and somewhat complicated to use a 64K RAM IC with part of it overlapping ROM. However, with the 64K chip coming into full production (a forecast of 140 million 64K RAM ICs in 1983) for use in minis and mainframes, we may expect to find them in frequent use in micros before long.

With all the address decoding on the chip, the design of the computer board is correspondingly simplified. It has been reported in New Scientist (8 July 1982) that the British firm Inmos has just produced its first 64K DRAM which shows a number of interesting features. One feature is that it automatically refreshes itself, so eliminating the need for special refresh circuitry on the computer board. Also, it operates twice as fast as the 4116.

Another feature is that the RAM carries eight spare rows of memory cells and eight spare columns. Making very complicated circuits on a single chip has the advantage that the connections between different units (eg between RAM and multiplexing and decoding circuits) are all on the chip and do not have to be taken out through terminal pins. This means that the IC need have fewer pins in proportion to the amount of circuitry it contains. Against this is the fact that as we increase the area of silicon on which the chip is made and as we increase the number of components put there, the chance of blemishes and faults rises steeply. It is common to manufacture dozens of chips on a single slice of silicon and, after testing them individually, to reject a high percentage. Obviously a high rejection rate puts up the final cost of the product. With eight spare rows and columns of memory cells, the spare ones can be connected in place of faulty ones after the RAM has been tested in manufacture. This means that the rejection rate falls and eventually the cost of the product can be reduced.

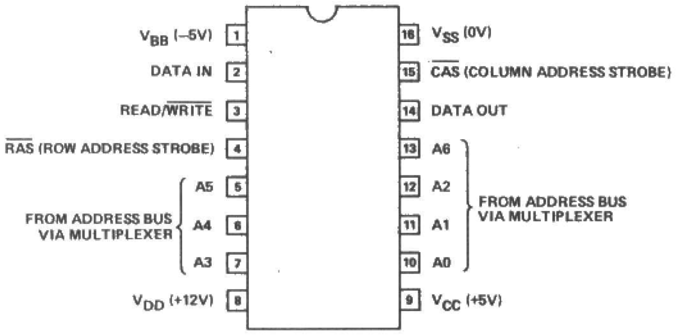

V_{BB} (−5V) 1
DATA IN 2
READ/$\overline{\mathrm{WRITE}}$ 3
$\overline{\mathrm{RAS}}$ (ROW ADDRESS STROBE) 4
A5 5
A4 6
A3 7
FROM ADDRESS BUS VIA MULTIPLEXER
V_{DD} (+12V) 8
16 V_{SS} (0V)
15 $\overline{\mathrm{CAS}}$ (COLUMN ADDRESS STROBE)
14 DATA OUT
13 A6
12 A2
11 A1
10 A0
FROM ADDRESS BUS VIA MULTIPLEXER
9 V_{CC} (+5V)

Fig. 11 (Above) Pin connections of the 4116 dynamic RAM.
Fig. 12 (Below) Block diagram of 16K of dynamic RAM.

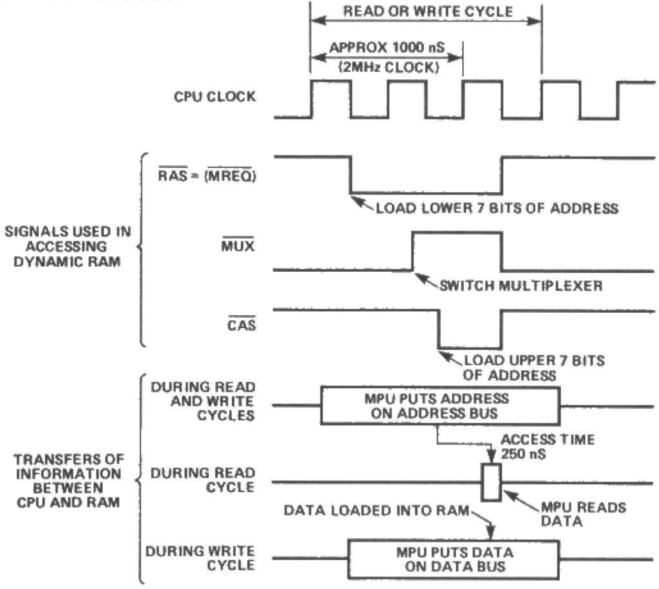
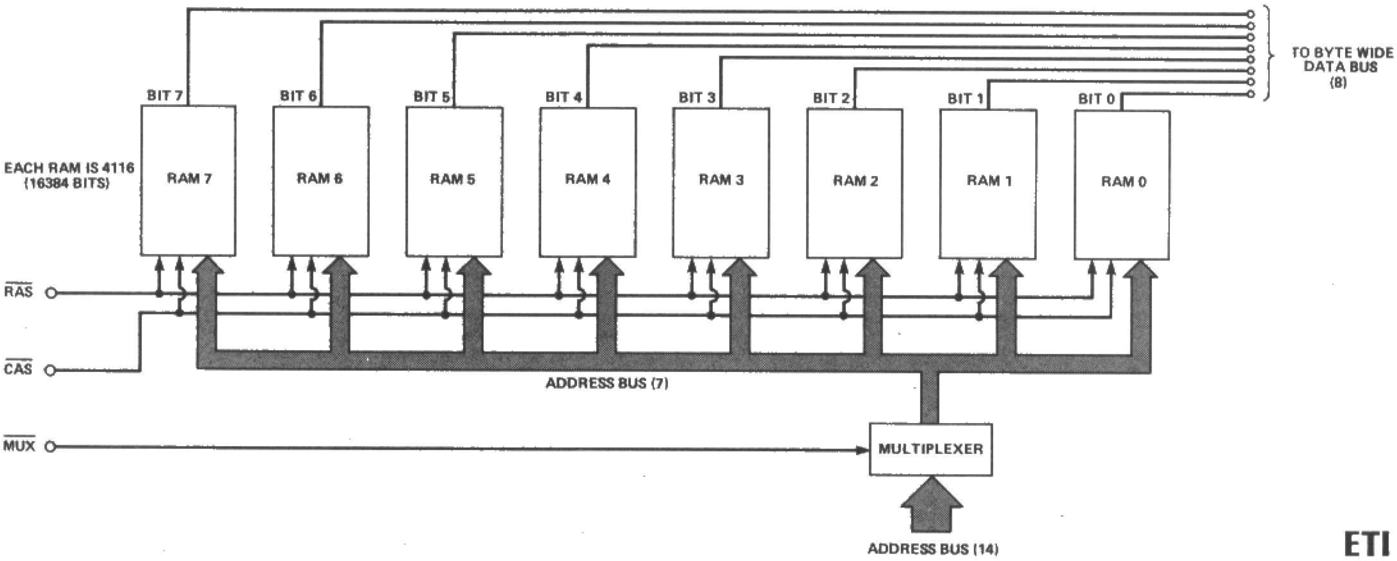

READ OR WRITE CYCLE
APPROX 1000 nS (2MHz CLOCK)
CPU CLOCK
SIGNALS USED IN ACCESSING DYNAMIC RAM
$\overline{\mathrm{RAS}}$ = ($\overline{\mathrm{MREQ}}$)
LOAD LOWER 7 BITS OF ADDRESS
MUX
SWITCH MULTIPLEXER
$\overline{\mathrm{CAS}}$
LOAD UPPER 7 BITS OF ADDRESS
TRANSFERS OF INFORMATION BETWEEN CPU AND RAM
DURING READ AND WRITE CYCLES
MPU PUTS ADDRESS ON ADDRESS BUS
ACCESS TIME 250 nS
DURING READ CYCLE
DATA LOADED INTO RAM
MPU READS DATA
DURING WRITE CYCLE
MPU PUTS DATA ON DATA BUS

Fig. 13 (Above) Reading or writing to dynamic RAM.



MESSAGE PANEL INTERFACE BOARD

A handful of TTL, a small PCB and a socket, and you and your ZX computer can go for a scroll down memory lane. Design and development by Rory Holmes.

The interface described in this article supplements the Message Panel character cards featured last month. It allows any number of linked character cards to be driven from either the Sinclair ZX81 or the ZX Spectrum computer. Using the program published in this article, repeating messages drawn from a 7 × 5 ASCII character set can be displayed with a variable scroll speed across the message cards.

Essentially the interface is an eight-bit output port for the ZX expansion bus, whose logic levels are translated from TTL to the 9 V CMOS logic levels. The interface can be used as a universal CMOS output port for Sinclair computers (CMOS with supply voltage below 10 V).

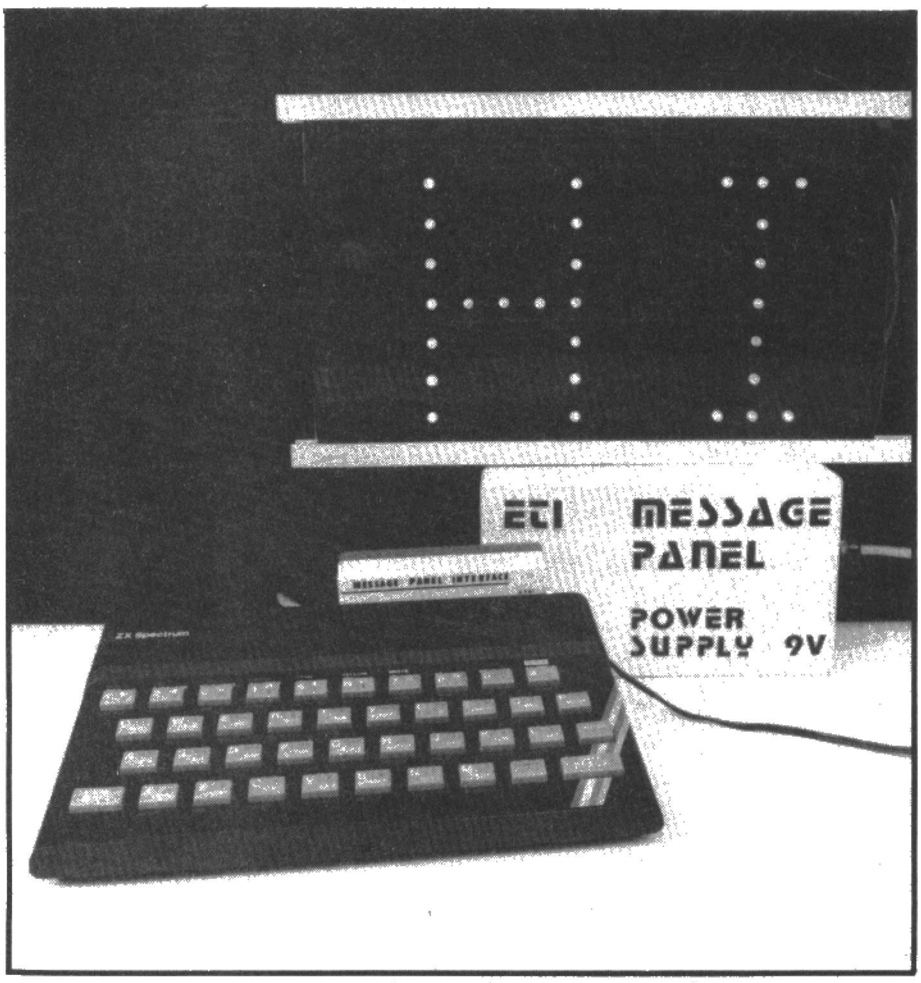
The port is memory mapped for the ZX81 and I/O mapped for the Spectrum; a DPDT slide switch is used to change between the two, though this may be replaced if desired by permanent links on the PCB.

In the interests of economy our circuit decodes only the top three address bits on the ZX81, placing the port over an 8K address range starting at 8192 decimal. Since this coincides with one of the 8K ROM 'echoes' a $\overline{\text{ROMCS}}$ signal is returned to the bus to de-select the ROM whenever the interface is addressed. Although the port responds to all the addresses in this 8K block it will not interfere with the basic memory or add-on RAM. With the Spectrum the port is I/O mapped at location 65503 and is accessible using the command OUT 65503,N. Again, it does not interfere with memory, and add-ons such as the printer may still be used.

Boxing Clever

The interface is built into a two part Vero case as shown in the photographs. An edge-connector protrudes through the front to plug directly into the Sinclair expansion bus. Correct location is achieved for both computers with a polarising key at position three (on the connector, that is, not the bus). The wire-wrap type of edge-connector socket that we have used also allows an edge-connect expansion plug to be soldered directly to the back of the PCB against the protruding pins, allowing the ZX bus to follow through the interface box. Other add-ons can then be simply plugged in at the back. A 10-way cable, either ribbon or multi-core, connects the interface output to the first Message Panel character card.

The character cards have seven CMOS data inputs for the shift registers and one CMOS clock line. They all require logic drive signals compatible with 9 V CMOS logic levels. The clock line is treated as the most significant data bit to make up the eight-bit control bus which goes to the interface along with the positive supply rail and earth. These



All wired up and ready to go — the complete Message Panel.

supply lines provide the CMOS interface logic voltages. A sequence of eight-bit numbers can completely control the Message Panel.

In order to keep down the size and cost of the board, we have resorted to a compromise with the TTL-to-CMOS level translation. Using open collector TTL with pull-up resistors, a 0 to 7 V logic swing is produced to drive the 9 V CMOS. This works fine for the shift register data inputs (7 V being above the CMOS switching threshold), but isn't suitable for the CLOCK line, because it drives the clock inputs of all the shift registers in parallel. For this reason a one-transistor buffer is used on the eighth output bit to provide a sufficiently low impedance, full 9 V swing, for driving the clock line reliably.

Construction

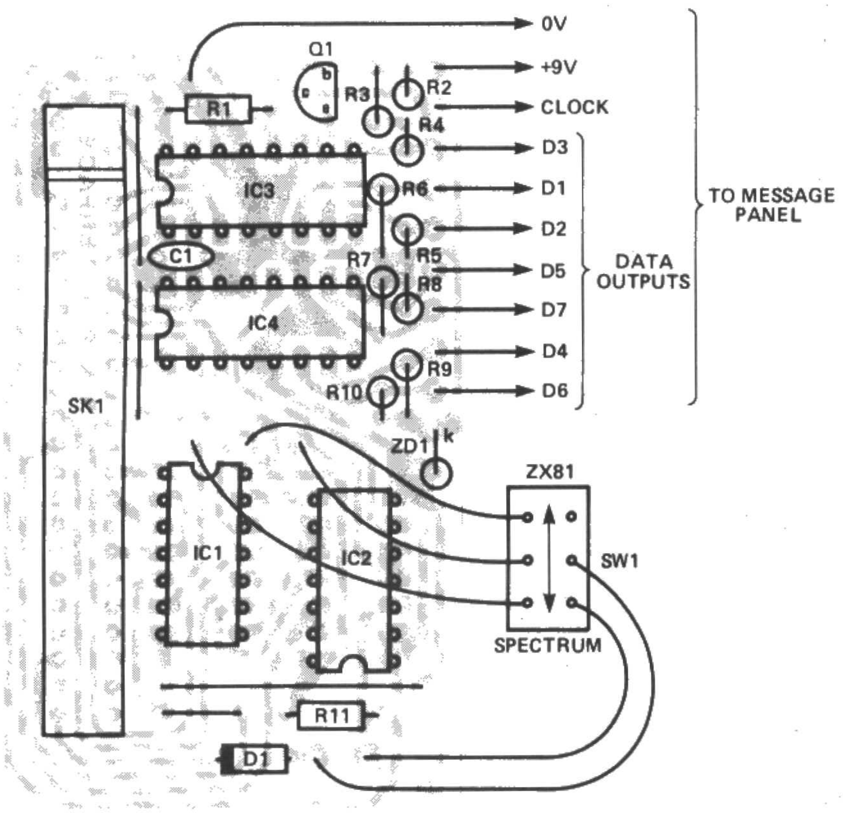
The interface is constructed on a PCB whose overlay is shown in Fig. 1. The PCB has been designed to take a 23-way double-sided edge-connector socket, which must have long wire-wrap pins to allow the connector to stand off from the board. The edge connector comes with a polarising key at position 3 and so must be fitted into the PCB the right way round. A 43-way connector could also be used, providing the unwanted ends are carefully sawn off so that the key remains in the same position. It's quite difficult to get all the edge connector pins through the PCB holes at once, but with the aid of a screwdriver and some patience it can be eventually be done. Before soldering the connector in place, ensure that it is square to the PCB, with the top edge being 21 mm from the component side of the board. This should leave the wire-wrap pins protruding about 2 mm from the track side of the board.

Fit the four links and IC sockets next, and then insert Veropins at all the connection points marked (they are also useful for connecting up to the slide switch). The vertical resistors can now be soldered in along with the other components, and finally the ICs can be plugged in, carefully observing their orientation. The DPDT slide switch should now be wired up with flying leads to the connection points as shown on the overlay.

Before final assembly the interface may be tested. Wire up the 0 V and 9 V Veropin connections to a PP3 9 V battery; this simulates the Message Panel power supply to determine the logic level output voltages. Now, simply plug the polarised edge connector into the back of your ZX81 or Spectrum computer. Switch on the computer, having first set the slide selector switch, and then monitor the data output pins with a voltmeter or scope. A logic low should be represented as 0 V while logic high will be about 6V8, but note that the data output pins are not in consecutive order.

In immediate mode, the OUT 65503, X command can be used for the Spectrum, and the POKE 8192, X command should be used on the ZX81. The value of X should appear as binary digits on the data outputs. For instance, POKE 8192,128 should result in the clock output pin going logic high and all the data pins going low. POKE 8192,3 will make the D1 and D2 outputs go to 6V8 (logic high), while all the other outputs remain at logic low.

A number of digital output patterns should be tested to ensure that all the output bits are working.



NOTE:
k = CATHODE

Fig. 1 Component overlay for the Message Panel interface board.

BUYLINES

Apart from the specialist hardware, nothing for this project should present undue problems. The 74LS TTL is now as common as dirt and can be obtained from such advertisers as Thames Valley Electronics, Cricklewood, Technomatic, Watford and Rapid Electronics. Wire-wrap edge connectors are sold by Timedata, 57 Swallowdale, Basildon, Essex, while the PCB can be obtained, as usual, from our PCB Service on page 91.

PARTS LIST

Resistors (all ¼W, 5%)	
R1	**10K**
R2	**1k0**
R3, 11	**470R**
R4-10	**22k**
Capacitors	
C1	**10n ceramic**
Semiconductors	
IC1	**74LS27**
IC2	**74LS00**
IC3, 4	**74LS170**
Q1	**BC184L**
D1	**1N4148**
ZD1	**6V8 400 mW zener**
Miscellaneous	
SW1	**DPDT miniature slide switch**
SK1	**23-way double-sided edge connector with wire-wrap pins, key at position 3 for ZX81; 23-way double-sided edge plug for optional expansion (see Buylines)**

PCB (see Buylines); Verocase (ref. 65-2514F); Veropins; nine-core screened cable.

When satisfied with the operation of the interface, the PCB should be assembled into its case; it has been designed to fit a small two section Vero case, order ref. 65-2514F. The slide switch is mounted through an appropriate hole at one end, while the nine-way multi-core cable enters the box at the other end (see the internal photographs showing the PCB mounted in the case). The screen of the nine-way cable is used to carry the 0 V line to the message panel, and therefore if ribbon cable is used instead it should have 10 ways. The 10 outputs are all wired directly, via the cable, to the corresponding connections on the Message Panel. The case lid must have a rectangular hole cut to allow the edge-connector to protrude as far as possible through the front. The board should be raised from the base of the box on spacers, so that it is firmly sandwiched between the lid and the spacers when the case halves are screwed together; we used four large stick-on rubber feet as the spacers, to give a compression fit. After restraining the nine-core cable with a cable-tie or similar, it should be wired to earth and the nine terminal pins, preferably using colour coding for the data bits. A nine-way D-type cannon connector plug was found ideal for terminating the far end of the cable (make sure the earth passes through the plug screen).

Setting Up The System

The system diagram of Fig. 3 shows how the separate parts are linked together to give a working Message Panel system. The 9 V power supply is the simple unregulated circuit shown last month. We mounted it in a separate box which plugs directly into the Message Panel via a two-way cable.

The program shown in Fig. 4 runs on a standard Sinclair Spectrum, and will allow messages entered on the keyboard to be displayed. It stores the character-generating data in a string array C$(7, 64) and uses this to display a message of any length entered in M$. The subroutine at line 3000 performs the data output and clocking of the message panel, with a variable scroll rate determined by the PAUSE statement. Subroutine 9000 sets up the character generator array C$ by using the Spectrum's ASCII characters to represent the data (this is done for convenience and to save memory space). The value returned for each character in

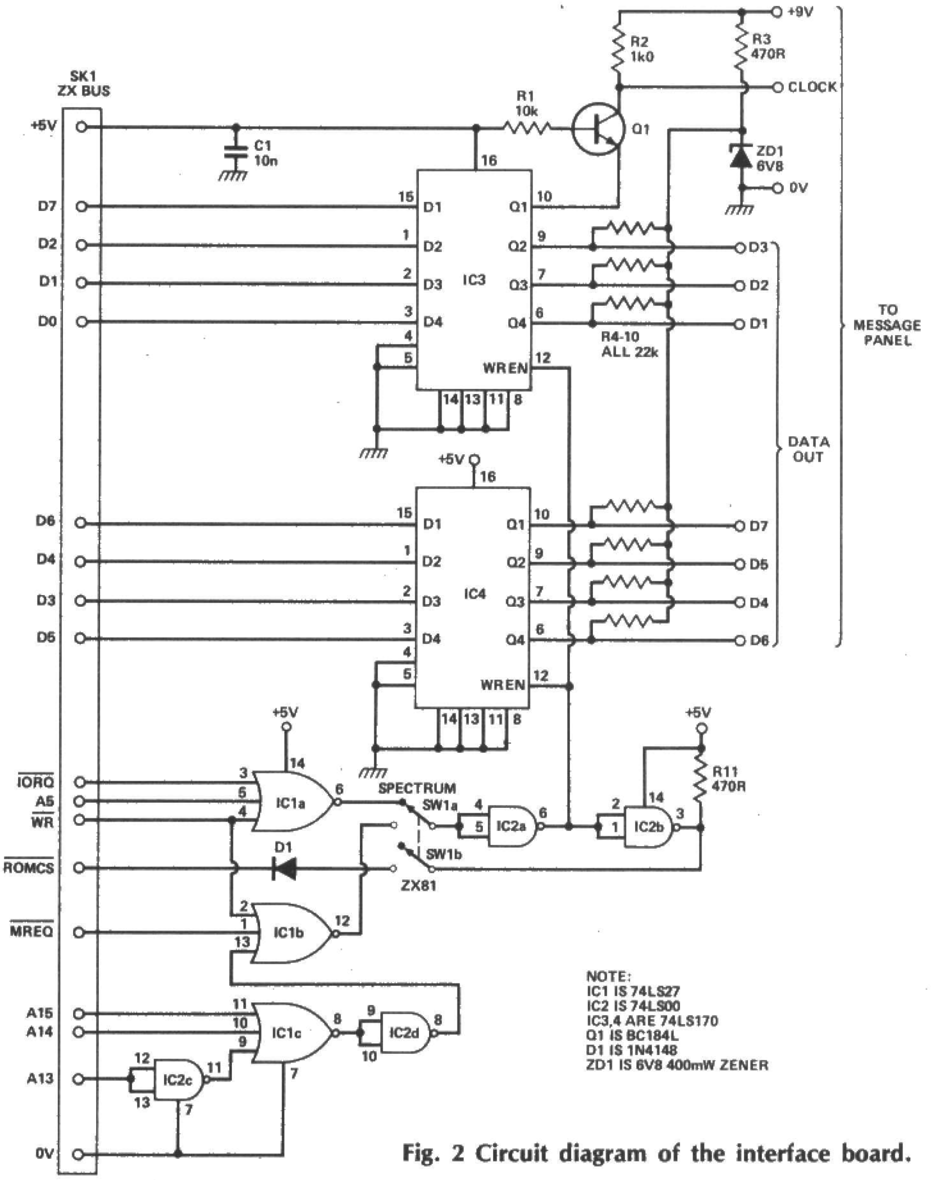


Fig. 2 Circuit diagram of the interface board.

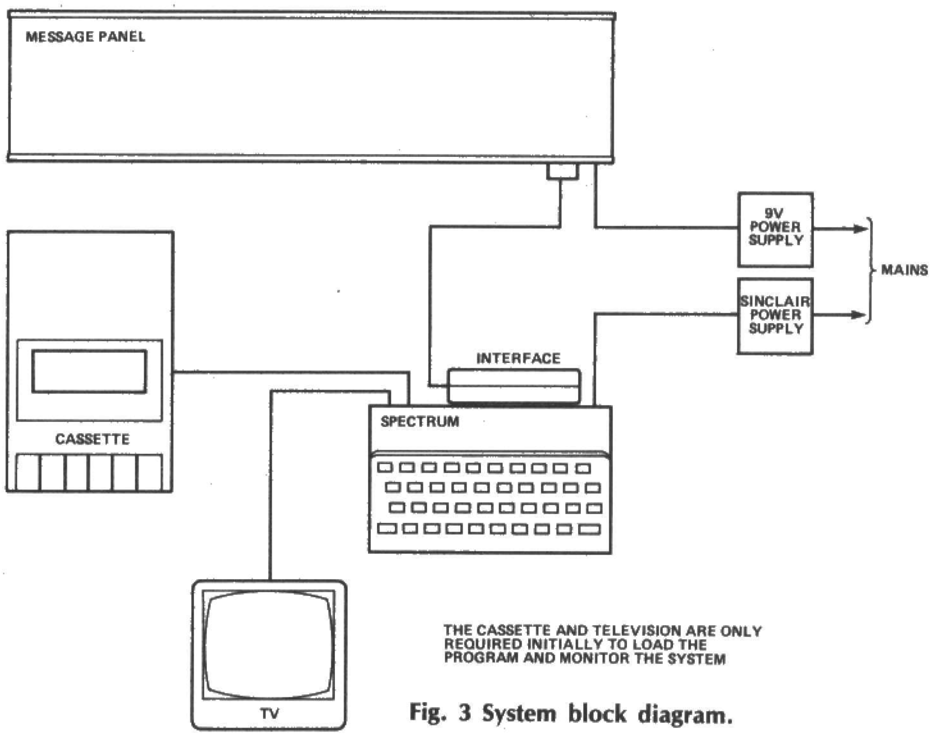

MESSAGE PANEL
9V
POWER
SUPPLY
SINCLAIR
POWER
SUPPLY
MAINS
INTERFACE
SPECTRUM
CASSETTE
TV
THE CASSETTE AND TELEVISION ARE ONLY
REQUIRED INITIALLY TO LOAD THE
PROGRAM AND MONITOR THE SYSTEM

Fig. 3 System block diagram.

HOW IT WORKS

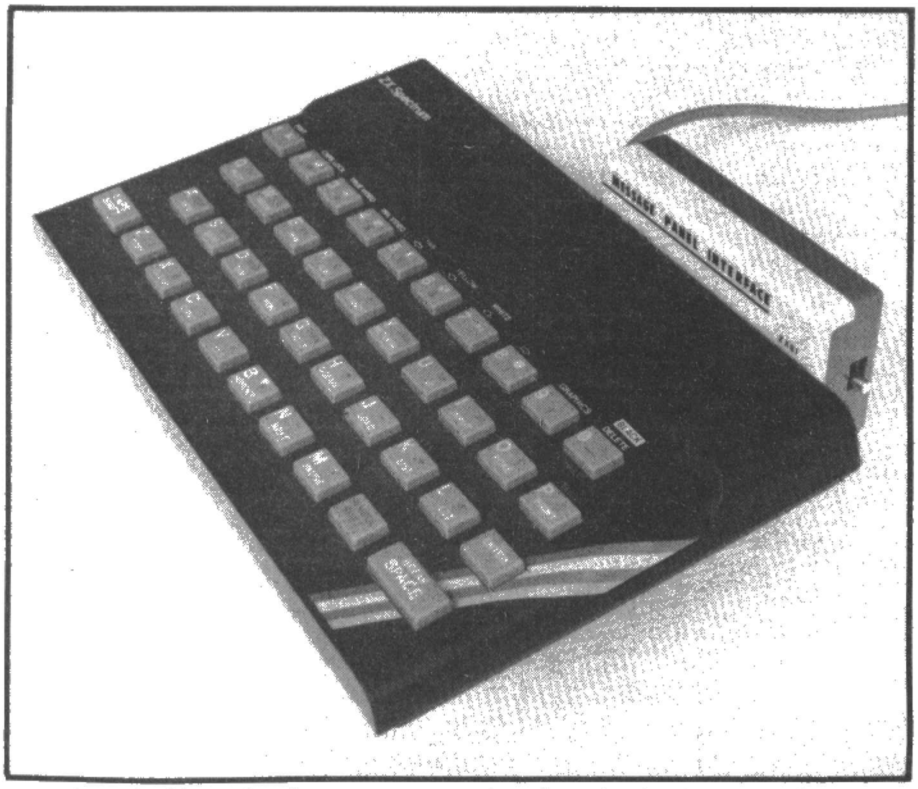
The port is essentially an eight-bit latch that will accept and store data from the ZX data bus as long as the address bus is sending the correct address to enable the latch. The latch is built from two four-bit registers wired in parallel, IC3 and IC4; they are actually 'four by four' register files (the 74LS170) of which only one four-bit latch is used. When the WRITE ENABLE input on pin 12 is taken low the latches will store the data on the D inputs; it then appears at the Q outputs.

The Q outputs are open collector types and they are used with pull-up resistors R4 to R10, thus increasing the available logic-level swing to match the CMOS inputs on the character cards. The maximum collector voltage allowed on the TTL Q outputs is 7 V and so the available swing is limited to 6V8 by the zener diode ZD1. R3 drops the 9 V CMOS positive rail voltage to supply the pull-up resistors. The logic swing of 0 to 6V8 is quite suitable for driving single CMOS inputs with up to 10 V on their positive rail supply (to achieve reliable switching from logic 0 to logic 1, CMOS needs an input of around 60% of the supply voltage). So the shift register data inputs will be reliably driven from these 'compromise' outputs. However, the CLOCK line on the message panel will need to drive every shift register IC that is being used; for this reason a single-transistor level-translator and buffer (Q1) has been used.

The address decoding is all achieved using IC1 (a triple three input NOR gate), and IC2 (quad NAND gates). Slide switch SW1 selects between memory-mapped decoding for the ZX81, via IC1b, or I/O mapped decoding for the Spectrum, via IC1a. When switched for the Spectrum the states of the bus lines IORQ (I/O request), A5 (address bit 5), and WR (write signal) are continuously monitored for logic lows. If they all go low together, then the Spectrum is performing an OUT 65503,X command, and the ouput of NOR gate IC1a will go high. This output is inverted by IC2a, which in turn enables the latches to store the data. An eight-bit data word can thus be updated into the latch at any time. The rest of the gates are effectively ignored, and as far as the Spectrum is concerned the A13, 14, and 15 inputs are connected to the wrong bus pins anyway.

When plugged into a ZX81, though, with the selector switch in its other position, these gates become usefully active. Here, address bits A14 and 15 must be logic low and A13 logic high to produce a high on the output of IC1c; this decodes the second 8K address region. The output of IC1c is inverted by IC2d and fed to one input of NOR gate IC1b. The other inputs monitor logic low states on the MREQ (memory request), and WR bus lines. Thus, IC1b's output will only go high when the ZX81 is performing a 'memory write' operation at an address location between 8192 and 16383. This output is fed to the latch enable via the selector switch and inverter as before. IC2b inverts and buffers the enable signal to drive the ROMCS line (linked up via SW1b). Whenever the interface is addressed this line will go high through diode D1 to switch off the 8K ROM.

The 70 mA or so of supply current for the TTL is taken directly from the 5 V supply rail on the ZX bus; C1 is included for on-board decoupling.



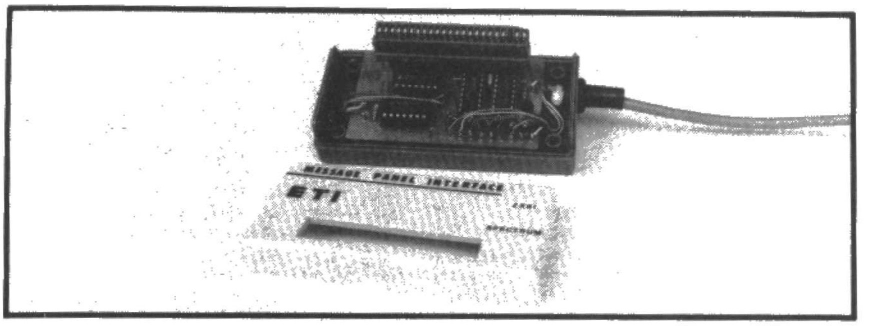
Like all good add-ons for the Spectrum, our interface simply plugs onto the expansion port.

```
   1 REM * MESSAGE PANEL PROGRAM
 *
   2 REM
   5 LET P=65503: LET CLK=128
  20 DIM C$(7,64)
  30 GO SUB 9000
  90 INPUT "SCROLL SPEED 0.5 TO
5 ?";S
 100 INPUT "YOUR MESSAGE ?";M$
 130 GO SUB 1000
 140 GO TO 130
1000 REM DISPLAY MESSAGE IN M$
1010 FOR K=1 TO LEN M$
1020 LET C=(CODE M$(K))-31
1030 FOR L=1 TO 7: LET B=CODE C$
(L,C)
1040 GO SUB 3000
1050 NEXT L
1060 NEXT K
1090 RETURN
3000 REM * OUTPUT PATTERN DATA
           TO PORT

3010 OUT P,B
3020 OUT P,B+CLK
3030 PAUSE S
3090 RETURN
9000 REM * INITIALIZE CHARACTER
           DATA

9010 LET C$(1)="      $t6        £
> Γ   '(a6      A 2!A>A©©>©  ©©©©>
©>©  ? ©c a"
9020 LET C$(2)="     w# I  A  X £
ABIA EJ II6[     I ©A©I A A@ @   A
 A E @     Q© A"
9030 LET C$(3)=" _   k V     >B £
A©II EI II6;    Yy IAAI A ©@ @   A
 D I©@£  xIA A©*"
9040 LET C$(4)="     :w‡d  A
>@II©EI I)      A IAAA I A@ @   A
 !)Q @     EA ©"
9050 LET C$(5)="       £P
  F6 90 6   A    >16 >A y© ?A@©©>
 ↑F   ? ©c C £"
9100 FOR I=6 TO 7: FOR J=1 TO 64
: LET C$(I,J)=CHR$ 0: NEXT J: NE
XT I
9200 DIM D(5): DIM N$(5,2,36)
9210 LET D(1)=31: LET D(2)=31: L
ET D(3)=26: LET D(4)=32: LET D(5
)=36
9220 LET N$(1,1)="ABCDHIJKLMNORT
UZ[\]↑£jtuwz|}"© ": LET N$(1,2)=
"@@@T@@@UH@H@@bXF@@@TB@bAGC@C@DH
"
9230 LET N$(2,1)="ABCFHIKLNPUX]↑
_£bgilnoqsuwyz}© ": LET N$(2,2)=
"@@GSG\NHHPTQHTbARIHHBBIIAXTDDB\
"
9240 LET N$(3,1)="ACDFHIJKNPUX]↑
_bgilnoqsxy}": LET N$(3,2)="@@@H
Gbb_HHRITTTQIHTLDIYPHH"
9250 LET N$(4,1)="ABCHJKLMNOPX[\
]↑_£bgilnoquwyz}© ": LET N$(4,2)
="@@G@\NH@H@DE@@bTHFRAHbBHIAXTDP
BH"
9260 LET N$(5,1)="ABCDEHIJKLMNOP
QRUXZ[\↑_£dgjqtuwz|"© ": LET N$(
5,2)="@@@TRB@@@UH@H@C@@PC↑@@T@@bA
@FbAGC@@DH"
9280 FOR I=1 TO 5: FOR J=1 TO D(
I)
9290 LET C$(I,(CODE N$(I,1,J)-64
))=CHR$ (CODE N$(I,2,J)-64)
9294 NEXT J: NEXT I
9900 RETURN
```

Fig. 4 Spectrum display program.

TABLE 1

CHARACTER		COLUMN 1	2	3	4	5
1		0	0	0	0	0
2	!	0	0	95	0	0
3	"	0	7	0	7	0
4	#	20	119	0	119	20
5	$	36	42	107	42	18
6	%	99	19	8	100	99
7	&	54	73	86	32	80
8	'	0	7	7	0	0
9	(	0	28	34	65	0
10	)	0	65	34	28	0
11	*	21	14	31	14	21
12	+	8	8	62	8	8
13	,	0	88	56	0	0
14	-	8	8	8	8	8
15	.	0	96	96	0	0
16	/	96	16	8	4	3
17	0	62	65	65	62	0
18	1	0	66	127	64	0
19	2	114	73	73	73	70
20	3	34	65	73	73	54
21	4	24	20	18	127	16
22	5	39	69	69	69	57
23	6	60	74	73	73	48
24	7	97	17	9	5	3
25	8	54	73	73	73	54
26	9	6	73	73	41	30
27	:	0	54	54	0	0
28	;	0	0	59	0	0
29	<	0	8	20	34	65
30	=	20	20	20	20	20
31	>	65	34	20	8	0
32	?	2	1	89	6	0
33	@	50	49	121	65	62
34	A	124	18	17	18	124
35	B	65	127	73	73	54
36	C	62	65	65	65	34
37	D	65	127	65	65	62
38	E	127	73	73	65	65
39	F	127	9	9	1	1
40	G	62	65	65	73	121
41	H	127	8	8	8	127
42	I	0	65	127	65	0
43	J	32	64	64	64	63
44	K	127	8	20	34	65
45	L	127	64	64	64	64
46	M	127	2	12	2	127
47	N	127	2	4	8	127
48	O	62	65	65	65	62
49	P	127	9	9	9	6
50	Q	62	65	81	33	94
51	R	127	9	25	41	70
52	S	34	69	73	81	34
53	T	1	1	127	1	1
54	U	63	64	64	64	63
55	V	7	24	96	24	7
56	W	127	32	16	32	127
57	X	99	20	8	20	99
58	Y	3	4	120	4	3
59	Z	97	81	73	69	67
60	[	0	127	65	65	0
61	\	3	4	8	16	96
62	]	0	65	65	127	0
63	↑	4	2	127	2	4
64	_	8	26	42	8	8



M$ is used to address a sub-string seven characters long in C$. The CODE value of each character in the sub-string corresponds to the binary pattern for each column of dots in a character on the character cards.

The program can easily be adapted for running on the ZX81 with extra RAM, but the character codes must be altered because the character set on the ZX81 does not have the same codes as the standard Spectrum ASCII character set. In the Spectrum program, a string array has been used for storing the pattern data merely to save space, and the string representation of this data must be changed to work with the ZX81's character codes. Table 1 provides all the eight bit numbers for each column of dots in each character of our standard character set, published last month. This table could be used directly as a numeric array or converted to a string array (as in C$(7, 64)) using the CHR$ equivalents.

The program can be altered in a variety of different ways; for example, so as to display messages stored in the program as literal strings and selectable on a menu basis. Other character symbols are easily programmed in by adding more data. Inverse characters can be obtained by inserting the line:

```
3005 LET B = 127— B.
```

Once the program is in the computer and running, the television and cassette recorder can be dispensed with, allowing the computer to drive just the message panel in a continuous loop.

At first sight it might seem impossible to make the display scroll backwards; after all, the shift registers used in the character cards are not bidirectional and can only clock data from right to left. However, there's a cunning programming trick that can be used to overcome this problem. Suppose the message you're displaying has n characters. Each character is five columns wide and the program in Fig. 4 inserts a gap of two columns between letters. Hence each 'character' is effectively seven columns wide. If we now cycle through a modified 'message output' loop (GOSUB 3000) in the program 7n—1 times, and do it fast enough, the display will appear to have shifted back by one column. To output the clock pulses fast enough will probably require a machine code routine rather than the BASIC program listed here, but by sending a burst of clock pulses, followed by a pause, another burst, a pause and so on, the required effect should be obtained.

Incidentally, to hire a commercial display will cost you anything up to £250 per week!

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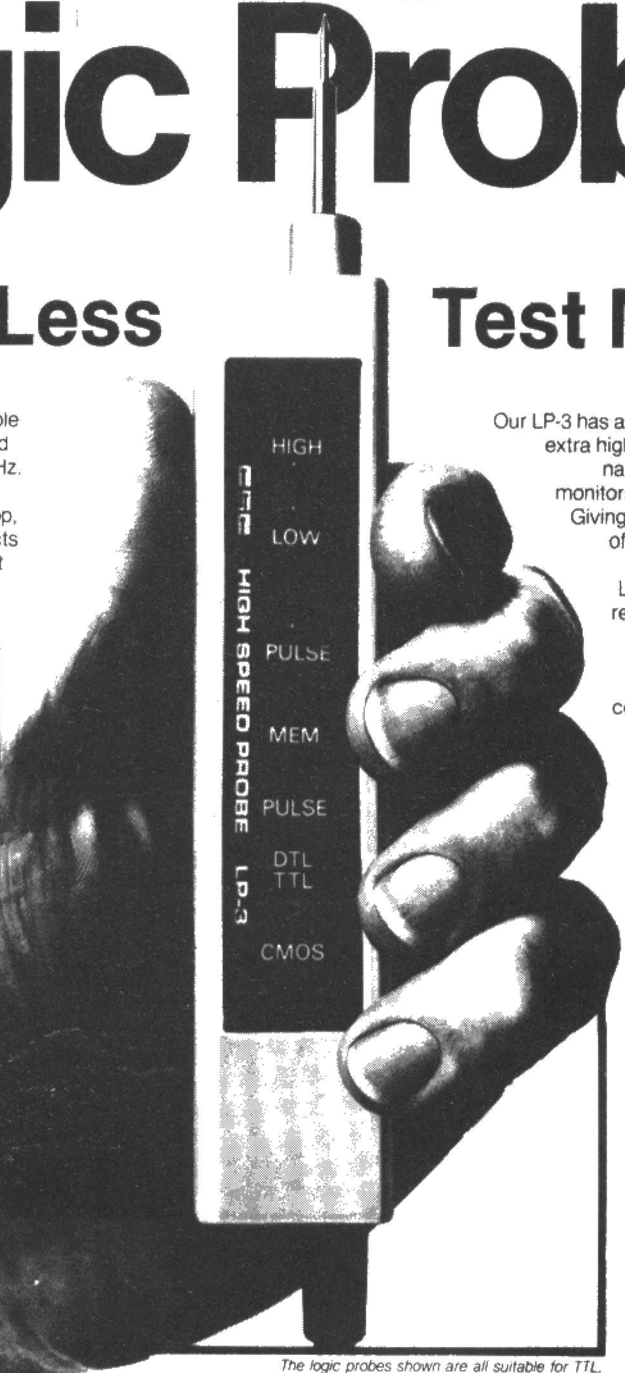

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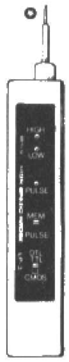

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The LP-1 has a minimum detachable pulse width of 50 nanoseconds and maximum input frequency of 10MHz. This 100 K ohm probe is an inexpensive workhorse for any shop, lab or field service tool kit. It detects high-speed pulse trains or one-shot events and stores pulse or level transistions, replacing separate level detectors, pulse detectors, pulse stretchers and pulse memory devices. All for less than the price of a DVM

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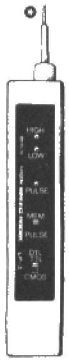

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The LP-2 performs the same basic functions as the LP-1, but, for slower-speed circuits and without pulse memory capability. Handling a minimum pulse width of 300 nanoseconds, this 300 K ohm probe is the economical way to test circuits up to 1.5 MHz. It detects pulse trains or single-shot events in TTL, DTL, HTL and CMOS circuits, replacing separate pulse detectors, pulse stretchers and mode state analysers.
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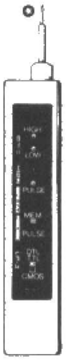

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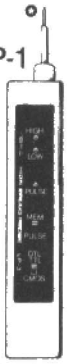

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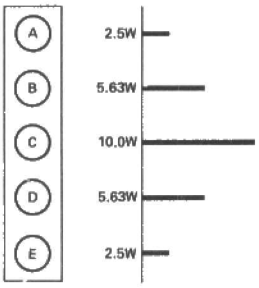
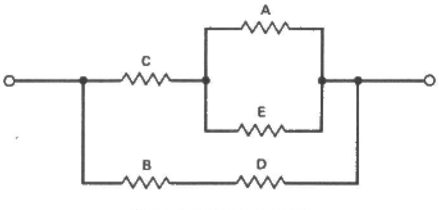
READ/WRITE

Letters for this page should be addressed to Read/Write at our Charing Cross Road address.

Dear Sir,

Having read the very interesting article on column loudspeaker design by David Hornsby (ETI May 82), I wonder why he did not use the following circuit:





(ALL SPEAKERS 8 OHMS)

It has, in my opinion, the considerable advantage of using only identical 8Ω speakers (instead of a mixture of 8Ω and 15Ω), and has an effective impedance of $6\cdot9\Omega$. The relative powers produced by the speakers are $2\cdot5$W, $5\cdot63$W and 10W, so although this does not give accurately linear grading, it comes close.

However, I wonder if linear grading is really what is required at all? I suspect that a Gaussian envelope ($\exp(-ax^2)$) is the ideal because its Fourier transform (also Gaussian) has no side lobes.

Yours faithfully,
M. R. Halse,
Kent

Yes, we agree that the circuit you give offers the advantage of using speakers all with the same impedance. However, you've got to remember that the speakers themselves are a poor approximation to an ideal continuously-varying line source, so niceties of the grading are already largely defeated. It's hard life, being a sound engineer.

Dear Sir,

Lucid Dream Induction Machine

I read the letter from Mark Botham in the August 1982 issue of Electronics Today, page 58, with great interest. Dr Hearne and I collaborated on the design requirements of lucid dream induction machines and related devices until about two years ago when, after a dispute about patent rights, we parted company. Dr Hearne applied for a patent on the device described (in Mark Botham's letter) on 19 January 1979 in his own name only. The crucial element in this version is the heat sensitive element attached to the nose. This method of measuring respiration has been around for some time although it seems that Dr Hearne did not know this when he came across it, independently of myself, and incorporated it into the general design we had both been working on.

No patent on this design has yet been granted in Britain, despite many published claims to the contrary (I have checked with the Patent Office, and Dr Hearne's application, GB 2039741 A, has not even received its substantive examination). The drawback with this design is that the person has to sleep with a lead attached to his nose which is tolerable for research purposes but seems likely to deter those who would use the device for amusement. There are other possible means of detecting dreaming sleep and gently alerting the dreamer to the fact that he is dreaming, but they tend to rely on uncomfortable connections which may become detached etc, not to mention the deterrent value of electric shocks, mild though they may be.

I am professionally engaged in research into lucid dreams and would be very interested to hear from anyone who could produce a machine that actually works. I think the reason that Mark Botham has not seen any test reports on this equipment in electronics magazines is that, again contrary to many exaggerated claims made on radio and TV etc, and although the device works well as a respiration monitor, trigger and stimulator, it is not so reliable as a means of inducing lucid dreams (this is not fault of the manufacturer) at least some of its partial success may be attributed to suggestion and sleep disturbance. No adequate scientific report has yet appeared to my knowledge in respect of any such device giving satisfactory evidence that vindicates the claims made for it. I have had hundreds of lucid dreams myself, and laboratory evidence has shown I can exert considerable control over these dreams. Nevertheless, I would say that such control is not easy to initiate or maintain and there is much development work ahead before such devices are really useful.

The method I use employs no apparatus but depends on waking after about five hours' sleep, walking around for about 15 minutes and then going back to sleep, telling myself that in my next dream I will realise I am dreaming and will take control. Using this method I have had dreams from which I have managed to communicate in Morse code. This is a very slow process and I am working on something rather better. If any readers would like to know more or to tell me about their spontaneous or induced lucid dreams (not ordinary dreams), they should write to me at the address given, and I would be grateful if a stamped addressed envelope is enclosed if a reply is required.

This is a new, exciting field and electronics will play a large part in it, but I must stress the importance of adequate tests to establish the effectiveness of these machines.

Yours faithfully,
Alan Worsley,
7 Salisbury Street,
Hull HU5 3EU.

OOPS

LOGIC LOCK (July 82). Several errors on this one; on the Parts List C12, 13 and 15 should be 2n2, not 2u2, and R13 should be 4M7. The foil pattern as printed has a track missing between pins 3 and 5 of IC4, and some boards from the PCB Service also have this fault; however the overlay is correct. RUGBY CLOCK (September 82). Type numbers were not given for Q1 and Q2; the former is a 2N3819, the latter a BC109. In Fig. 5 IC6c pin 3 is joined to pin 6 of IC4, and pins 9 and 12 of IC8a, 8b should be joined to pin 4 of IC8d. In Fig. 6, RESET on IC15 and IORQ on IC19 should have bars over them (active low) and pin 22 of IC17 is 'INTERRUPT OUT'. In Fig. 7 the junction of R21 and C11 should be joined to IC20c pin 7. ACTIVE SPEAKER (September 82). Two minor mistakes; There is no IMF 28/30; the bass driver is in fact the 8/28BR. Also Fig. 7 omits the link from IC2 pin 4 to R2/C7/C9.

ETI

AUDIOPHILE

This month, Ron Harris concludes the report that nearly finished him off — listening tests on the heavyweights of super-fi.

The End. All over. Amplifiers unwired from switching boxes and preamp allowed mercifully to cool towards room temperature. The comparison is completed at last. Sony and Trio blew it — no sign was seen of either the Esprit or L08C, despite repeated cursings and threats. Hence no mention can, or shall, be made of what are reputedly good pieces of machinery.

Of those that *had* faced up to life, therefore, there remained the three principles and thus the primary reason for this whole complicated exercise: Class A versus MOSFET versus Magnetic. As a yardstick by which to judge the performance of these high-power, high-price speaker-drivers, I included the Crimson 1100 in the group tests. The level of the comparative excellence — or otherwise — can thus be gauged by reference to the Crimson results, obtained under identical conditions.

Last month's technical results showed little difference between the main amps in terms of power output, etc. There would appear to be hope, therefore, that we can aspire to the ideal situation of being able to say that operating principle is irrelevant. After all, regardless of how the amplifier achieves the result, if it were indistinguishable from real life (hah!), then we would have a perfect amplifier.

How far away from this unobtainable Utopian ideal the art remains can be judged from the need for different manufacturers to choose *totally* different design concepts in an attempt to reach a common end. Would that it were that one solution offered a close enough approach, so that all else could be considered mere detail!

Listen with ETI

Devising a programme to show up differences in subjective testing is, of necessity, far from straightforward. However, as all the amps are of comparable power, it is a fairly simple matter to adjust the preamp gain to give an identical voltage across the load from each amplifier.

Exactly how, and for what, the panel should be asked to mark the resulting sound is another matter. After much debate — and a final act of dictatorial aggression by yours truly — the parameters listed in Table One were chosen. I flatly refused to include such things as 'musicality' as in my opinion they are nothing more than an unscientific attempt to avoid a straight answer! Yes, the final nine that we used *are* subjective and capable of being misinterpreted. However, as long as the participants in the experiment are clear as to what the term implies within the bounds of the exercise, then they are valid.

(God help me, this article is going to illicit some stinking letters — I can see it now. There must be hundreds of people dancing up and down with rage all across the UK by now. Patience is all I ask. That and a little licence.)

The final programme settled upon was to be as follows — there would be an overall group comparison test, including the Crimson 1100, which would use the Shure V15V as a source and would require the panel to mark each unit for the following parameters: (i) treble extension (ii) treble clarity (iii) mid-range detail (iv) neutrality (v) stereo imaging (vi) transient handling (vii) bass extension (viii) bass detail (ix) overall presentation of programme.

The comparisons would be carried out without the panel being aware of which amp was playing at any one time. The same material would be used for each unit. Marks to be awarded out of a maximum of 31.

Table One is the collated and averaged marks for each amp, from the seven sets of results.

A second set of tests would be conducted, involving straight A–B tests of all units except the Crimson. A different set of criteria would be required to be marked this time, although the overall effect would be the same — one wins, one loses. Table Two lists out the results.

Just to make things interesting, I changed the pickup cartridge to a Dynavector Karat Ruby (without telling the panel) for this second set of tests! It is equally as good as the Shure, but has a radically different character and thus serves to produce a different emphasis of the amplifiers' characteristics.

As the Karat was kept in place for all the tests in this group, its use could have had no effect on the relative results: I was satisfied that it matched all the units equally well in its own way.

As I had had time to listen to all the amps at some length, I excluded myself from the panel. I worked the box of tricks instead. It would have been unfair of me, having already formed my opinions, to have taken part. Besides *someone* had to push the buttons and change the discs!

Sound Results

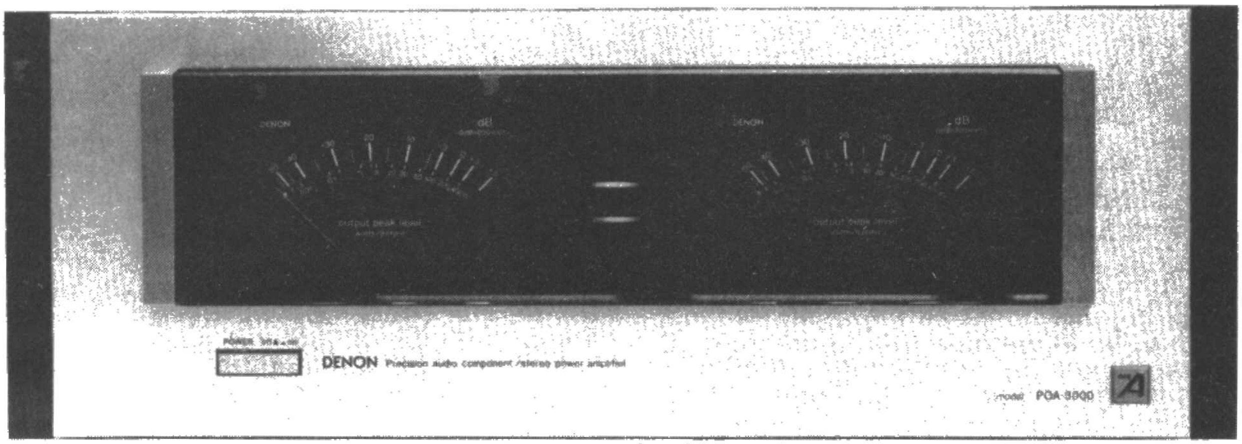
As you can see from the results tables, some definite preferences emerged. The Denon finished up clear of the

Table 1

	Carver M-400	Denon POA 3000	Hitachi 9500	Hitachi 7500 II	Crimson 1100
Treble extensions	23	27	25	21	21
Treble clarity	21	28	26	22	21
Mid-range detail	20	27	24	22	24
Neutrality	25	26	26	26	24
Stereo imaging	24	26	27	26	23
Transient portrayal	28	28	23	19	17
Bass extension	24	24	22	24	20
Bass detail	18	24	21	22	18
Sub-total	183	210	194	182	168
Overall presentation	24	27	25	24	21

Table 1 Results for the group listening tests. The mark in each column is out of a possible maximum of 31 (except for the sub-total).

➧



The Denon POA 3000 — the ultimate champ-amp?

rest on very nearly all the tests and in my opinion it deserved to do so. What *was* surprising, though, is that only two of the seven panel members could consistently pick out the Denon correctly. One of these always marked 31/31 and other marked it down!!! 'Too clinical' was the reason offered under subsequent interrogation in the local alcoholic vending place. When asked if this meant if he would prefer to be operated on with a blunt scalpel (not *too* sharp?), he failed to see the connection. Some people have about as much sense of humour as a dead fish. (After this appears there will be one hi-fi dealer in North London that I will not *dare* venture into, other than fully armed.)

The individual nature of the units involved militated against a long series of comparisons, because it would have not taken long before the panel began to identify the amps — thus destroying the impartiallity guaranteed by obscurity. I think had we continued the tests any longer, that would almost certainly have been the case.

The Denon POA 3000 is a fine piece of Class-A engineering. It has all the virtues of the mode, clean and clear power and finely etched detail, while not suffering from the usual drawback of low power.

Against this, the Carver M-400 offered an exciting presentation, startling transient handling — and a less precise presentation. The Hitachi 9500 II could show its effortless power production — despite the lower rating, very smooth mid-range — and (very) slightly booming upper bass registers.

On the basis of the tests overall, if we total up all the points gained we would arrive at the following league table:

1.	Denon POA 3000	85%
2.	Hitachi 9500 II	78%
3.	Carver M-400	74% (74.4%)
4.	Hitachi 7500 II (dual)	74% (73.6%)
5.	Crimson 1100	60%

These are simply percentages of total possible marks scored across the first set of listening tests. Including the second set produces:

1.	Denon POA 3000	85%
2.	Hitachi 9500 II	80%
3.	Carver M-400	78%

for the three principal units. And that is probably a fair reflection of how they did overall!

It is worth noting, though, how close the 'doubled-up' bridged 7500 II's came to equalling the 9500 II in a straight A–B test. In the group test, there is little to choose between these and the Carver M-400. It would be a matter of personal choice which you nominated as the 'better'. Thus, one clear conclusion is that if you already have a 7500, or are thinking of buying one, then the best possible upgrade — bearing in mind price — would be a second 7500! Watch the speaker impedance though, as this amp does get a mite temperamental on low loads.

We were going to run further M-400 versus 7500 II comparisons, but Carver's publicity people snatched away the Cube before we could complete these.

A MOSFET for all Seasons?

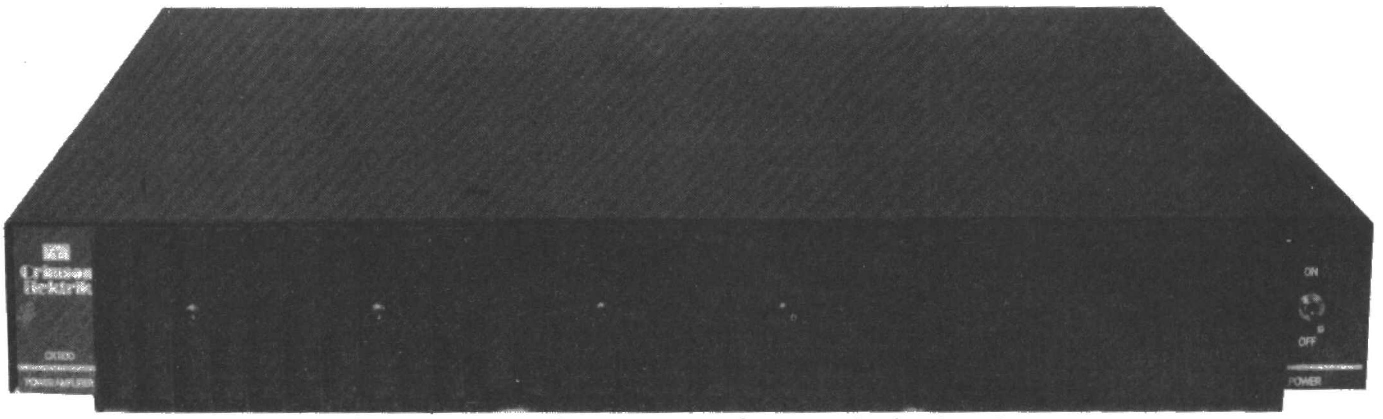
The 9500 II is an impressive piece of engineering. Sound from this massive unit was a fine vindication of the MOSFET principle and would appeal to many very strongly. MOSFETS have often been compared to valve amps, due to their similar overload behaviour, and the 9500 II *does* have the valve-like virtue of a smooth and open mid-range. It misses out on all the horrendous valve faults, however, like poor bass and the dreaded microphony.

Microphony in valves: the tendency of a sealed glass tube to allow modulation of the electron beam within by an ambient sound field, due to physical movement of the anode, cathode and grids. Result: false 'depth' and 'warmth' due to added reverberation. If you want the effect, buy a spring-line. If you don't, use transistor (or MOSFET!) amps.

Table 2

	A	B	A	B	A	B	A	B
	Carver v	Denon	Denon v	9500	9500 v	Carver	9500 v	7500 II
Cymbols	24	27	26	24	26	24	27	27
Female voice	22	23	24	24	26	23	26	25
Acoustic guitar	28	26	26	26	27	28	26	22
Choir	24	26	26	26	24	23	22	22
Orchestra	25	26	27	24	26	24	23	24
Trumpet	28	28	27	26	27	29	27	26
Group	27	24	27	26	26	26	26	24
Bass guitar	28	28	26	27	28	27	28	25
Total	206	208	209	203	209	204	205	195

Table 2 Results for the A–B tests; again, marks are out of 31.


The Crimson Elektrik 1100 — a worthy contender for the price.

Conclusions

What to say? Easier to decide what *not* to! Probably the easiest way out is to list:

1. The Denon POA 3000 was audibly superior to other units in the tests. It costs considerably more to own, but portrays all the virtues of Class-A amplifiers to perfection.
2. The Carver M-400 is an individual and interesting design. It did not, in our opinion, sound as neutral as the other units.
3. The Hitachi HMA 9500 II and 7500 II (bridged) MOSFET amps offer excellent value for money, refined engineering and a very good sound quality.
4. Considering its price the Crimson 1100, used as a yardstick here, performed well although it was outclassed by the Denon and the Hitachi 9500. It is a viable alternative to the Carver if the power output is not a consideration.
5. Further tests — against such as the Status units — would be necessary to determine the exact position of the Denon within the market place.

And for my Next Trick. . . .

Next issue sees the start of a new series-within-a-series, with Audiophile's Sound Thinking No. 1 — Pickup Resonances. This is an attempt to take some of the hype and implied mystery away from some of the least understood areas of hi-fi. We won't be dealing with basics — ETI readers should know all that stuff already — but rather the small but important effects brought to light by improved techniques and technology. Could be interesting. I hope.

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LOW LEAKAGE All single ended
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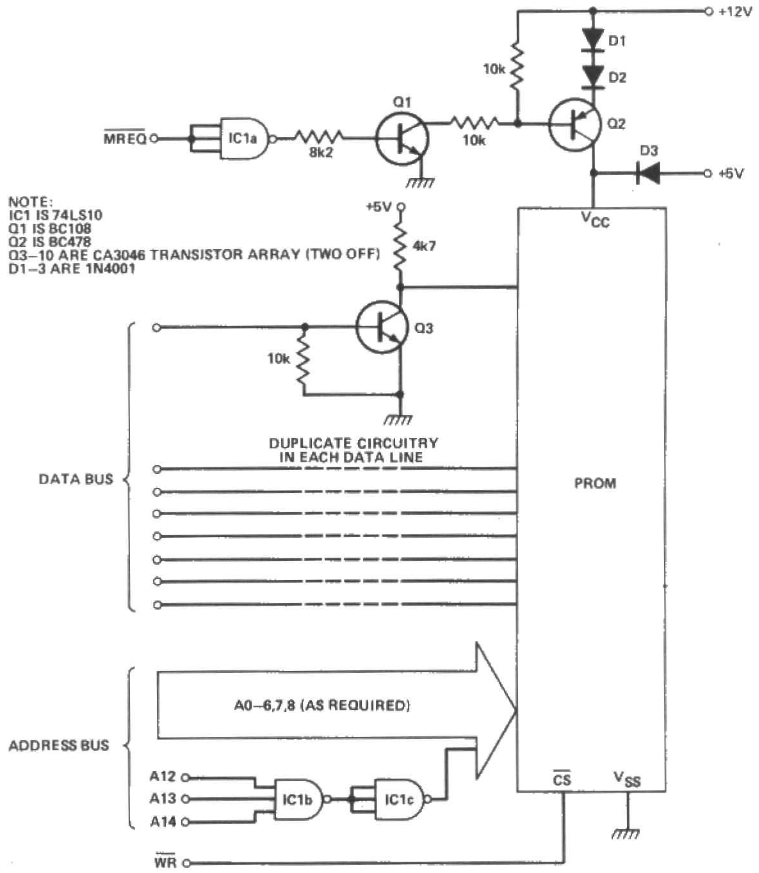
PROM Blowing by Computer

L.N. Owen, Wolverhampton

Fig. 1



NOTE:
IC1 IS 74LS10
Q1 IS BC108
Q2 IS BC478
Q3–10 ARE CA3046 TRANSISTOR ARRAY (TWO OFF)
D1–3 ARE 1N4001

Much attention has been given to EPROMs and EPROM programmers but little regard has been paid to their poor relation — the fusible-link PROM. These devices can often provide short cuts in circuit-building by replacing complete logic gate networks and thus reducing board area and power consumption. The fusible-link PROM is probably the nearest thing the hobbyist can obtain to his own design of integrated circuit.

Any type of computer can be used as long as the timing sequence is complied with — the prototype used a ZX81 and an SGS/ATES CLZ80. Only 1K of memory is required. Several types of PROM are available; this design caters for the following:

SN74S188, SN74S288 (32 × 8 bit)
SN74S287, SN74S387 (256 × 4 bit)
SN74S470, SN74S471 (256 × 8 bit)
SN74S472, SN74S473 (512 × 8 bit)

The circuit diagram is given in Fig. 1. This simple arrangement requires only one logic chip and two transistor arrays. Signals A12-A14 are decoded and inverted by the 74LS10 and thus provide the starting address of 26624 for the programming routine. The other gate is arranged as an inverter so as to produce MREQ at the base of Q1. To blow a PROM simply POKE the address (plus 26624) with the required data; to read it, have a PEEK (with +12 V disconnected).

The whole process is a memory write cycle with a modified MREQ signal; the timing diagram is given in Fig. 2. The sequence is thus: the address is placed onto the address bus, then the MREQ line is taken low and inverted by the NAND gate, causing the transistors Q1 and Q2 to supply about 10V5 to the programming pin (usually V$_{CC}$). The data bus is then loaded, after which the WR line is activated, thus blowing the PROM at the stated address with the stated data. The transistor arrays invert the data inputs, thus providing sinks for the programming pulse — they also act as protection devices for the computer. When the PROM is in the READ mode the 12 V supply is switched to 5 V.

Construction is very straightforward. If you intend blowing a lot of PROMs regularly then it may well be advisable to invest in zero insertion force sockets. One word of warning — a blown PROM is a dedicated animal and there is no question of 'unblowing' or perhaps 'sucking' it.

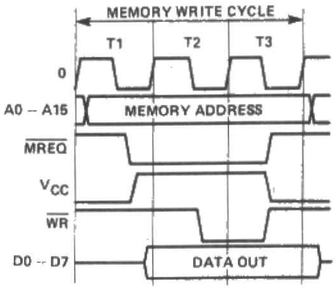


Fig. 2

Tech-Tips is an ideas forum and is not aimed at the beginner. We regret we cannot answer queries on these items. ITI is prepared to consider circuits or ideas submitted by readers for this page. All items used will be paid for at a competitive rate.

Drawings should be as clear as possible and the text should be typed. Text and drawings must be on separate sheets. Circuits must not be subject to copyright. Items for consideration should be sent to ETI TECH-TIPS, Electronics Today International, 145 Charing Cross Road, London WC2H 0EE.

Rotary Combination Lock

Chris Pearce, Middlesex

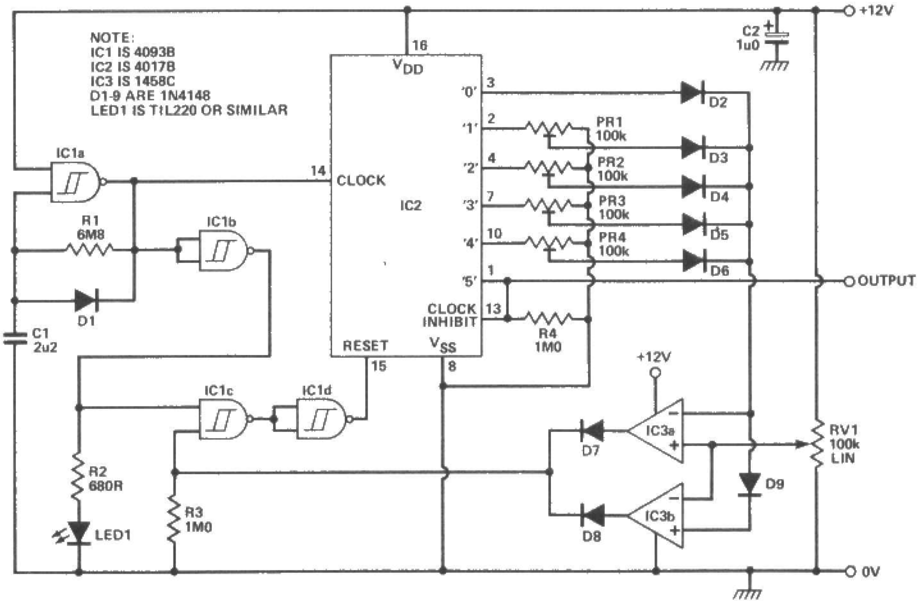
There are many circuits for push-button and rotary switch combination locks, but this circuit uses a potentiometer to enter the four-digit code (easily expanded to eight). LED1 flashes approximately every 2 seconds. To enter the code, the potentiometer must be turned to the first digit for the duration of one flash, then moved to the next digit, ready for the next flash, and so on until the code is entered. If a wrong number is entered at any time the lock will reset and the code must be re-entered.

RV1 should be set up so that it can point to a number between 1 and 10. As a 12 V supply was used, '1' corresponds to 2 V, '2 to 3 V, and so on. Circuit operation is as follows: IC1a and C1, R1, D1 form an oscillator which provides clock pulses for the circuit timing. This clock pulse drives IC2 and is also inverted to drive LED1 and the reset logic.

Assuming IC2 is reset and the code is '1234', a high will appear at IC2 pin 3, which corresponds to a count of '0'. On receiving the next clock pulse, the high will move to count '1' (pin 2). This will drive PR1, and thus feed a voltage to the window comparator IC3. D9 sets the window width at 0V6. As the first digit of the code is '1', which corresponds to 2V, PR1 will be set to 2V9, allowing for 0V6 dropped across D3, and thus setting the upper window limit to 2V3 and the lower to 1V7. If, when the LED flashes, the potentiometer is set to within the limits, the comparator output will be low and IC2 cannot be reset. On the next clock pulse IC2 will move to count '2' ready for the next digit and so on.

If the potentiometer is outside the limit ie the wrong number, the comparator output will be high and IC2 will be reset when the LED flashes. If the correct code is entered the clock of IC2 will be inhibited via pin 13 and the output will be high. To set the lock the potentiometer is moved off the last digit.

C1 should not be electrolytic. C2 provides decoupling and should be placed near IC3. The chance of breaking the four digit code in any one attempt is 1 in 10,000, and 1 in 100,000,000 for an eight digit code.



Computer Keyboard Encoder

Michael Jones, Dorset

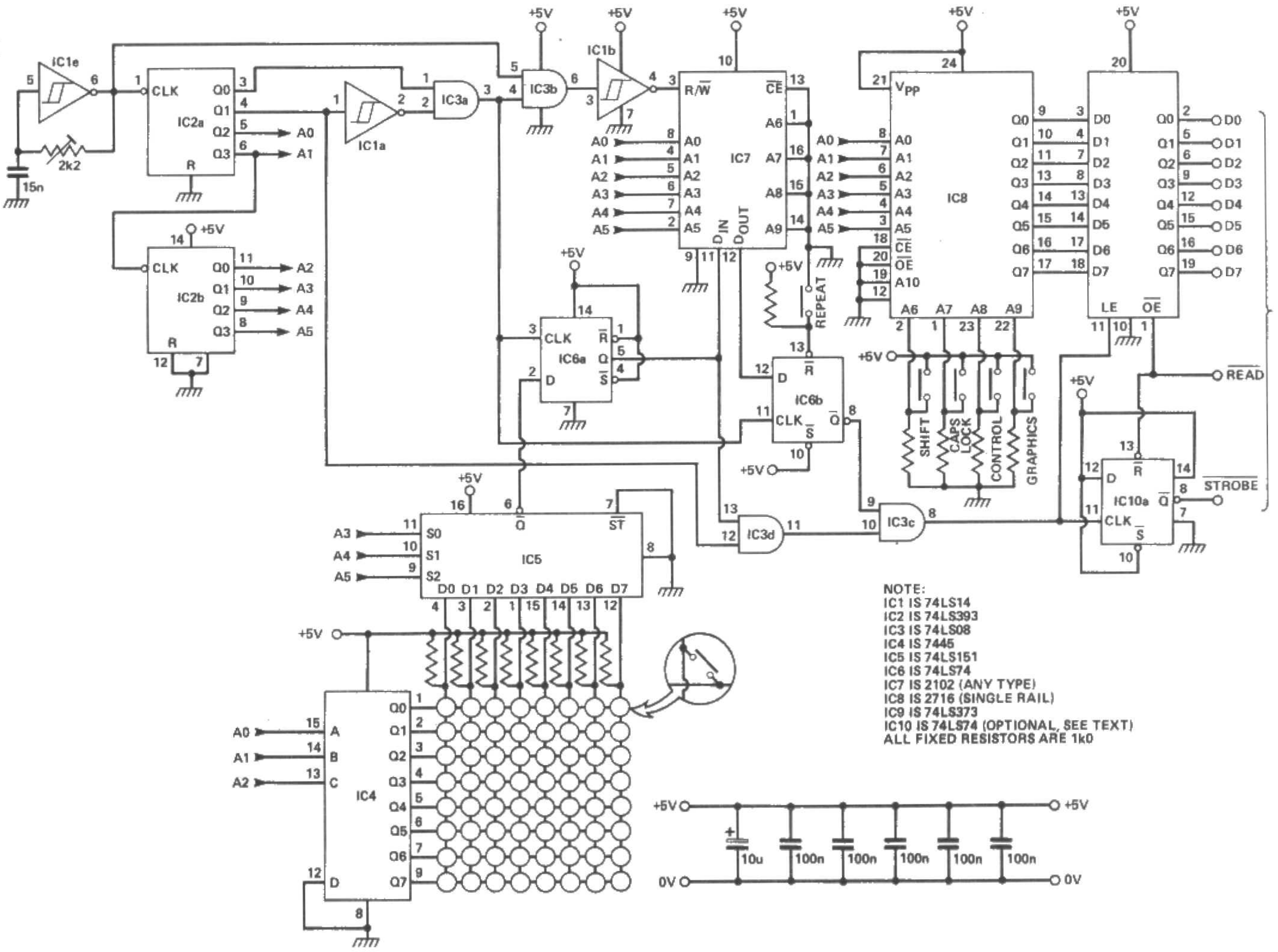
This circuit will encode a full size computer keyboard into ASCII or any other code the user requires. As it stands it handles 64 keys, plus shift, control, caps lock and graphics, although the circuit is easily expanded to cater for more. All the keys are debounced and full n-key rollover is provided. Instead of the auto-repeat found on some keyboards, this circuit provides for a separate 'repeat' key, pressed simultaneously with the required key.

Interface to the computer is via eight tri-state data lines, which may be connected directly to the computer's data bus, and two control lines. STROBE is a negative true signal output by the keyboard to inform the computer that data is available. IC10 latches it until the data is read, essential for the polling software used in most small computers; if, however, your keyboard software is interrupt-driven, IC10 is unnecessary and may be omitted, a short positive true pulse (typically 200 uS) being available on pin 8 of IC3c. READ is a negative true signal output by the computer to activate the outputs of IC9 and clear the STROBE latch. If the data is to be continuously output to an existing buffer then pin 1 of IC9 may be tied low, but pin 13 of IC10 must still have the equivalent of the READ signal. Spare inverters from IC1 are available to invert any of these signals if required. Only a + 5 V supply is needed, to normal TTL specifications.

The circuit operates in four 'cycles' defined by Q0 and Q1 of IC2a; a half-cycle is also obtained from the input clock. At the start of cycle 0 the upper counter lines (labelled A0 to A5) are incremented; these are used to select a key from the multiplexed array as well as selecting a corresponding address in the RAM (IC7) and the EPROM (IC8). The RAM is used to record the status of each key, enabling rollover. The EPROM selects the code to be sent to the computer; it must therefore be programmed with the desired codes in advance. The four keys (such as 'shift') select a different block of addresses in the EPROM to give alternative codes.

At the start of cycle 1 the status of the key is latched by IC6a and the previous status, from the RAM, is latched by IC6b. During cycle 1½ the new status is written to the RAM. During cycles 2 and 3 the new and old status are compared and, if appropriate, the data from the EPROM is latched and the STROBE line activated.

The preset on the clock generator (IC1c) can be used to adjust the scan frequency which determines the maximum key bounce permissible (one scan period) and the repeat frequency.

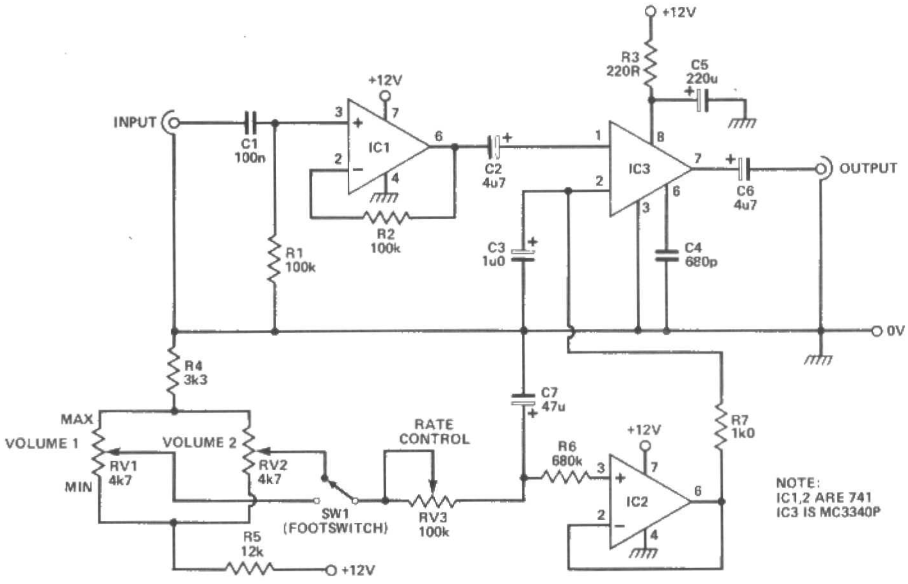


Switched Guitar Volume

R. D. Pearson, Sheffield

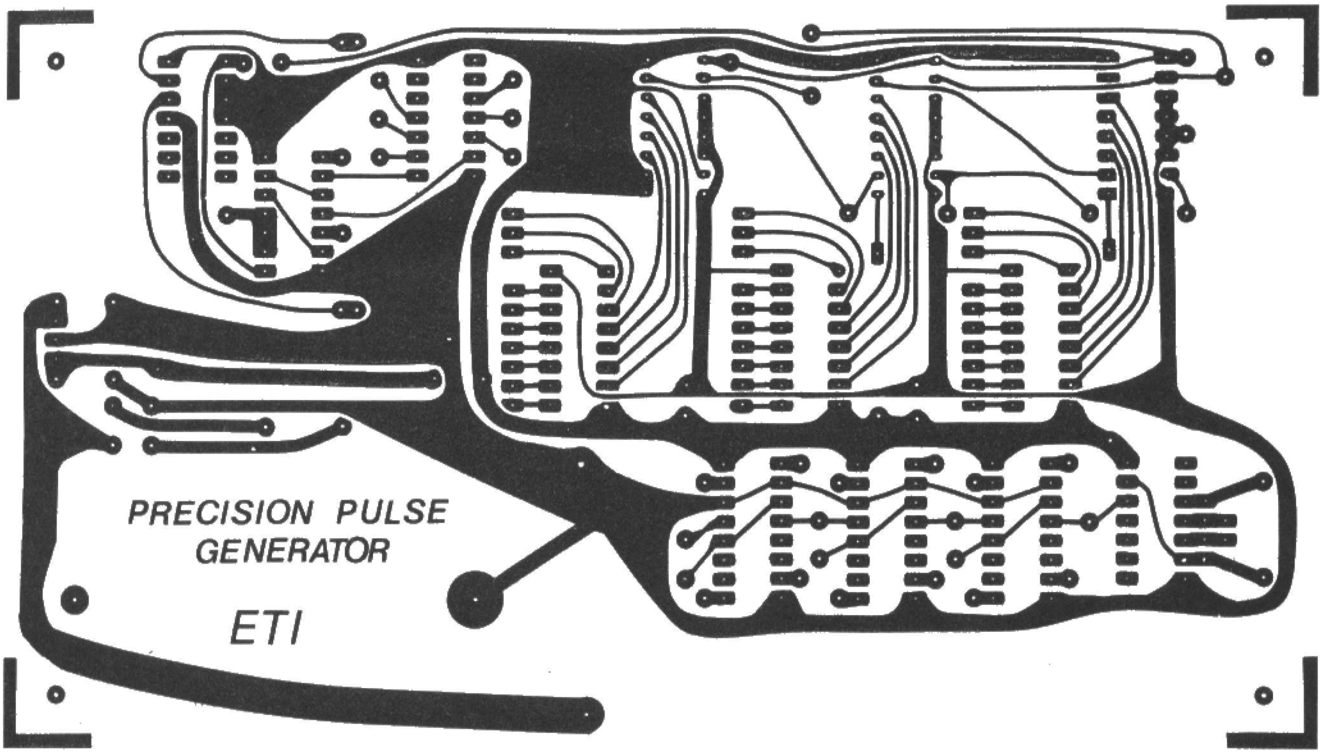
It is often useful for guitarists, especially on stage, to be able to change the volume of their instrument while playing, without having to bother about twiddling volume controls. This circuit makes this possible by switching between two preset levels set by RV1 and RV2. In addition, the output level can be made to fade up or down between the two preset levels at a preset rate set by RV3. Fading is done smoothly and without any crackles and clicks since there are no mechanical controls (ie switches and pots) in the signal path. All the guitarist has to do, having set the controls, is to kick the footswitch

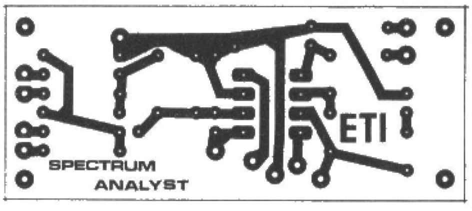
The input signal, having been buffered by IC1, is fed into the electronic attenuator IC3. The gain of IC3 is dependent upon the potential at pin 2. This is determined by the voltage across C7 which is buffered by the voltage follower, IC2. The voltage across C7 is set by the potential at the wipers of RV1 or RV2, depending on the setting of the footswitch. The rate at which the voltage across C7 changes, and hence the fading speed, is set by RV3.

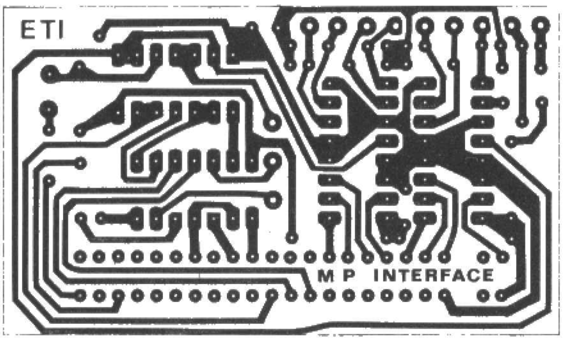


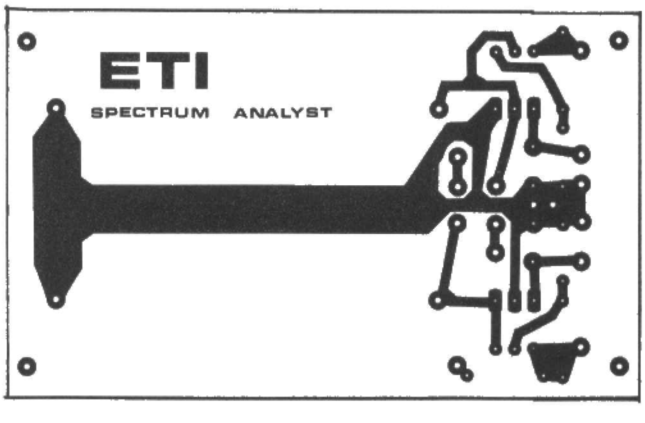
A ± 12 V power supply is required. This should be well regulated and free of ripple if a mains supply is used. The circuit is best built in a metal case as these are strong and reduce hum and RF pickup.

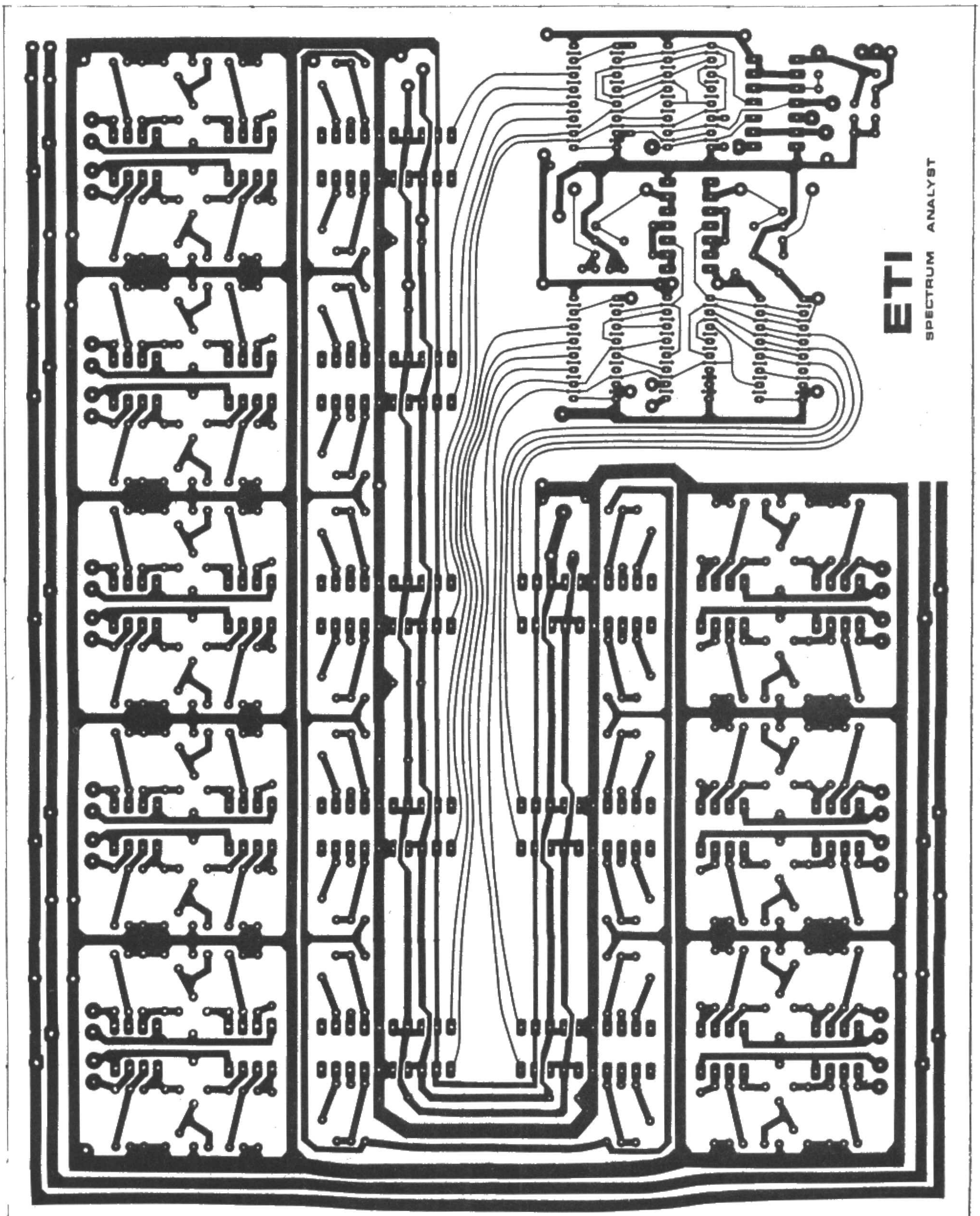
PCB FOIL PATTERNS







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In addition to the PCBs for this month's projects, we are making available some of the more popular designs from our recent past. See the list below for details. Please note that NO OTHER BOARDS ARE AVAILABLE. If it's not listed, we don't have it!

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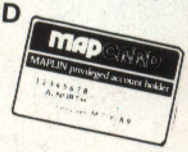

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**Projects for book 4 were in an advanced state at the time of writing, but contents may change prior to publication (due 14th Aug 1982).*

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